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Future Developments in Semiconductors

Oldenburg, July 11th 2003

Dr. Sönke Mehrgardt
Chief Technology Officer
InfineonTechnologies AG

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Future Developments in Semiconductors

Basics	• The Semiconductor Market • Moore‘s Law
Three barriers	• Lithography • Low-k • High-k
Outlook	• Future Technologies
Applications	• Biochips • Power Supply

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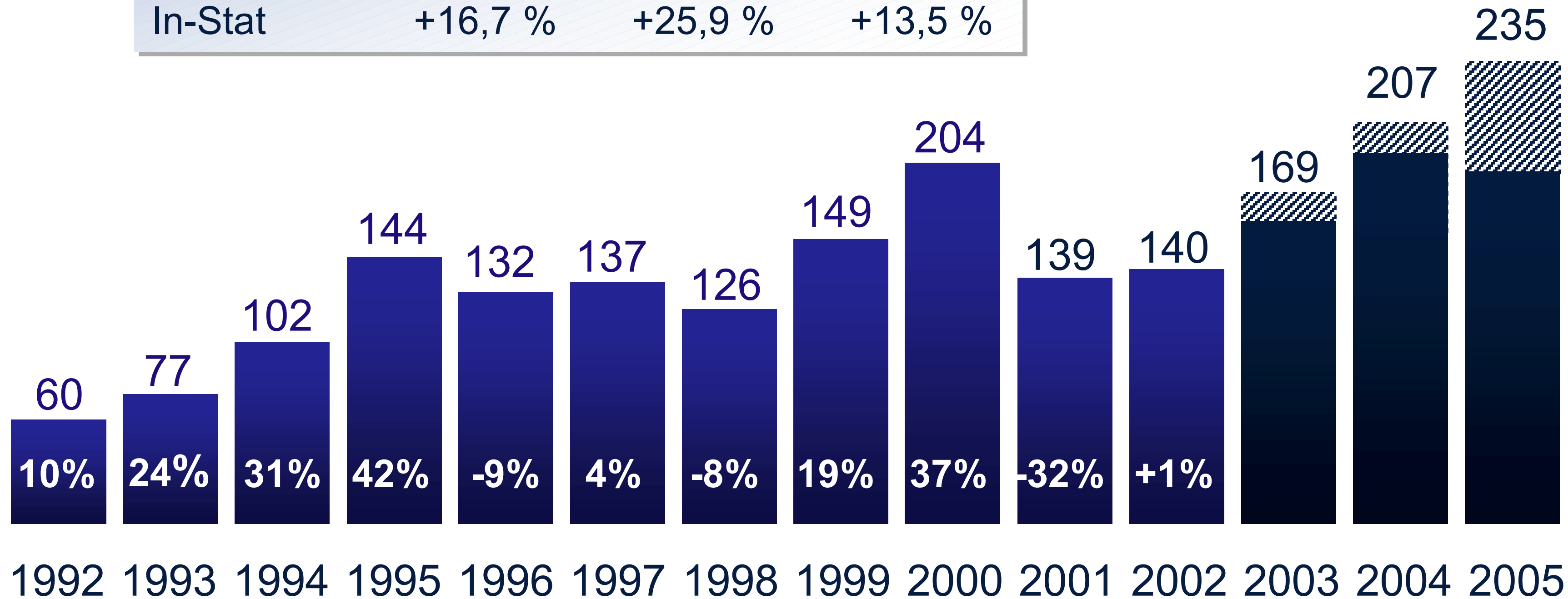
The Semiconductor Market

Source: WSTS

Forecast	2003	2004	2005
IC Insights	+15,0 %	+26,0 %	- 11,0 %
Dataquest	+ 8,9 %	+27,8 %	+19,2 %
SIA	+19,8 %	+21,7 %	0 %
WSTS	+14,1 %	+19,2 %	+ 2,6 %
In-Stat	+16,7 %	+25,9 %	+13,5 %

(Billion US $)



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The Semiconductor Market

Our Industry is pretty large, …

… but even larger are

Wal-Mart	$220 Billion in 2002	(„Big Karstadt“)
Exxon	$205 Billion in 2002	(Oil)

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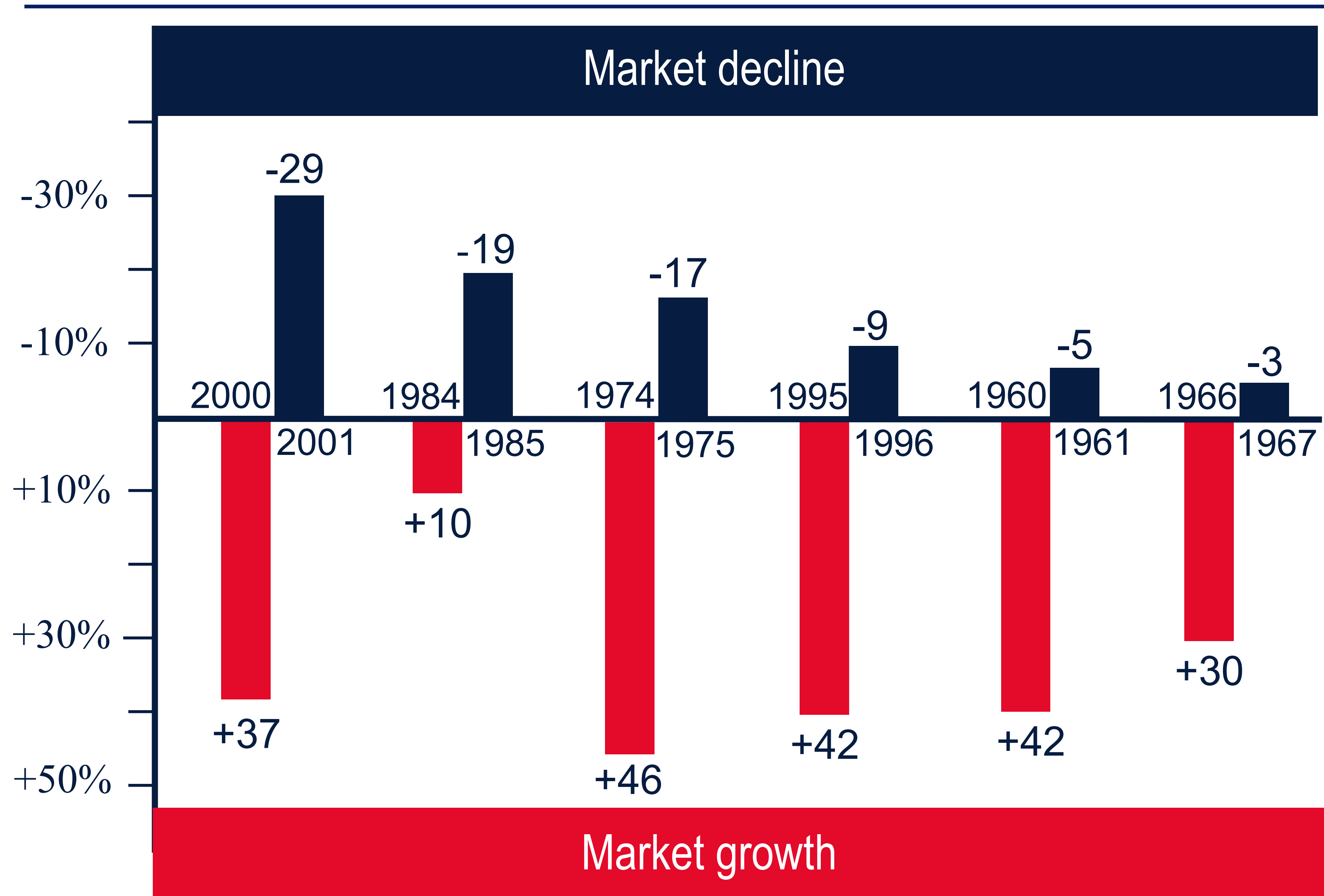
The worst cycles in four decades of semiconductors



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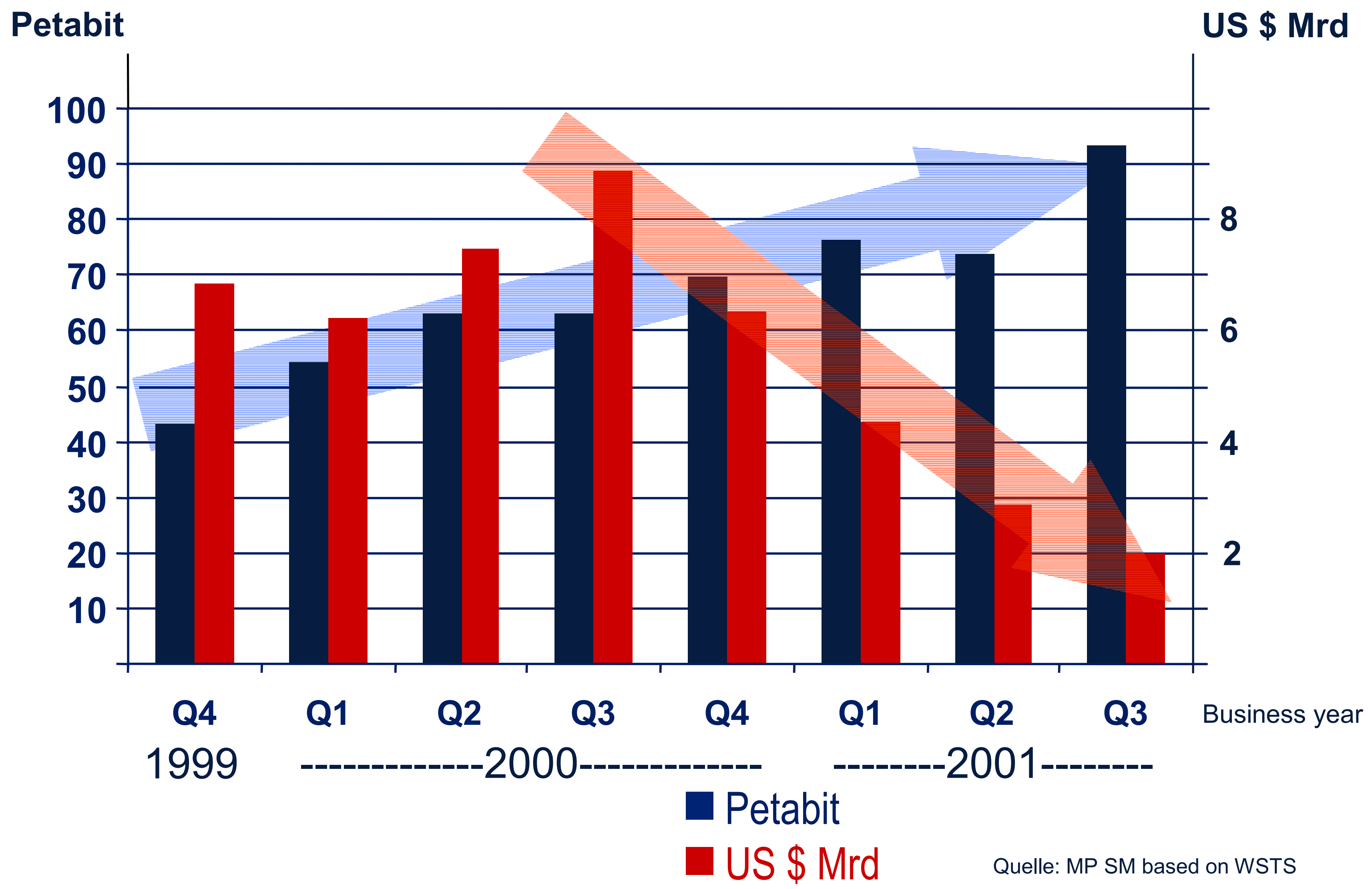
DRAM – Sales in bit und US $



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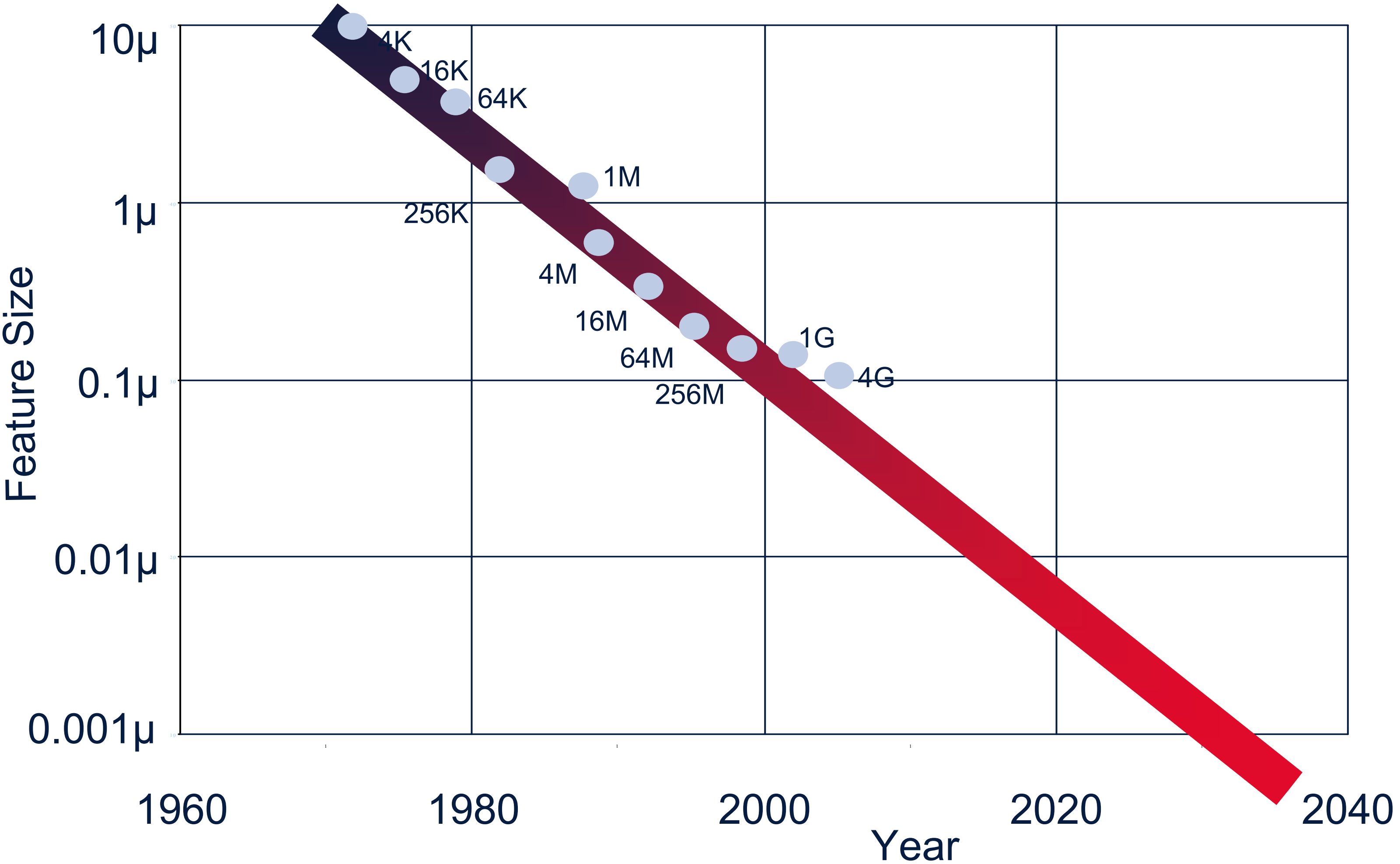
40 Years Going Strong - 40 Years to Go Much Stronger?

- Semiconductors have developed dramatically for over 40 years
- The technology development was breathtaking and has even accelerated recently
- However: More and more tough barriers come into sight (e.g. the atoms!)

Can we keep the development speed??

Exponential Improvements - Feature Size



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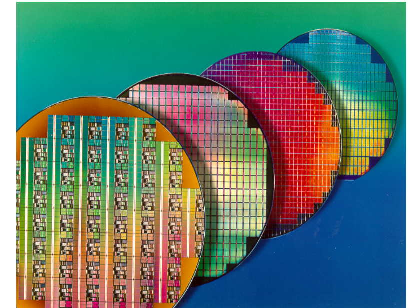
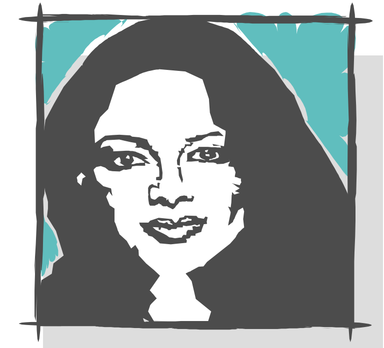
Are There Limits in Semiconductors?

Example - 4 Gbit DRAM (approx. 2005):



- 250,000 text pages or 10 h music
- 1,000 Billion atoms/bit

Comparison:



- 10 Billion atoms/bit: Human brain
- 20 atoms/bit: Genetic information

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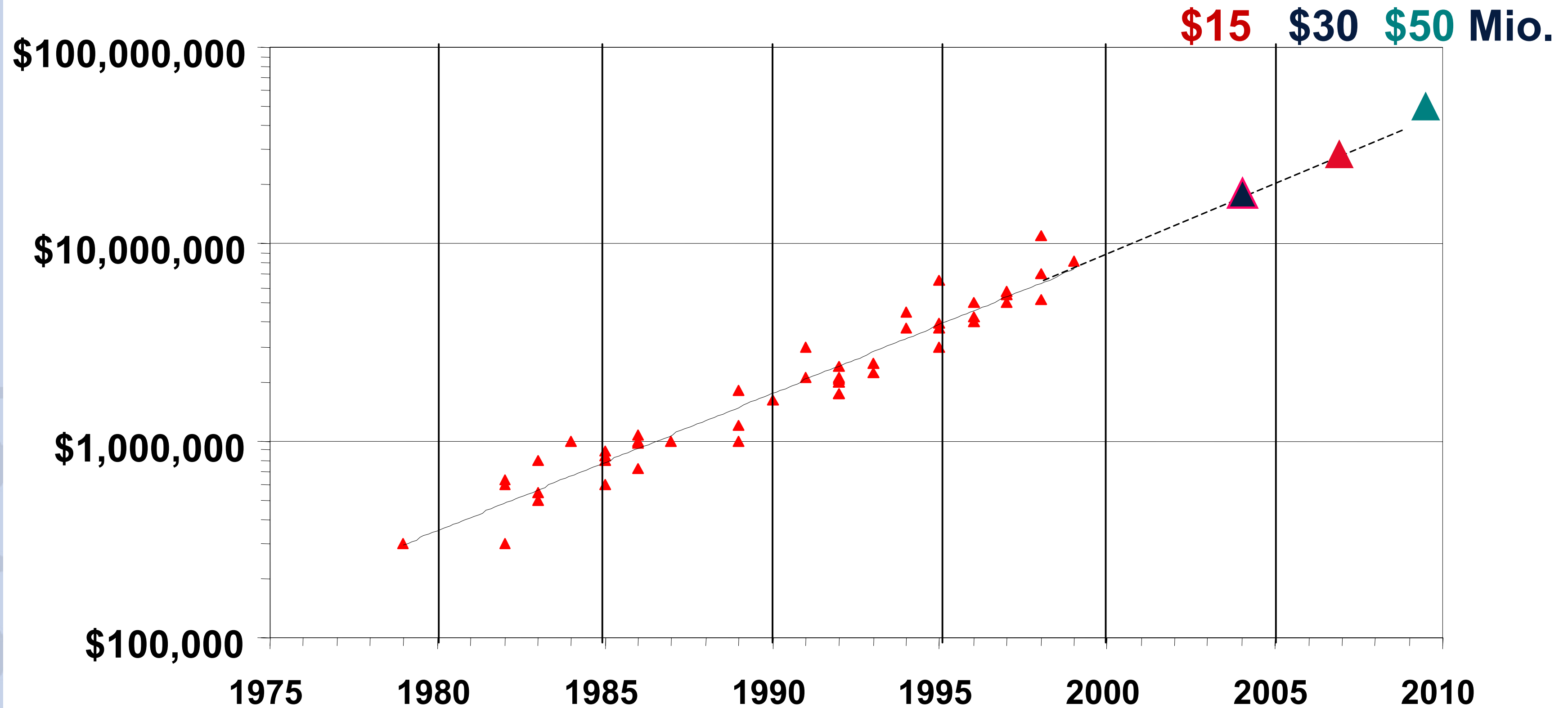
But: Production Equipment becomes extremely expensive!



… and very, very big!

Lithographie: 157nm Stepper

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Moore‘s Law

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“Moore's Law”

- The improvements result from three effects

  1/3 gain from increased chip size: chip size increasing exponentially

  1/3 gain from lithography: minimum feature sizes decreasing exponentially

  1/3 gain from circuit and design innovation (“circuit cleverness”):

  “There is no room left to squeeze anything out by being clever. Going forward from here we have to depend on two size factors - bigger dice and finer dimensions.”

  (Gordon E. Moore, Proc. IEDM, 1975, p.11)

- Prediction 1975

  Circuit density or capacity of semiconductor devices doubles every eighteen months or quadruples every three years

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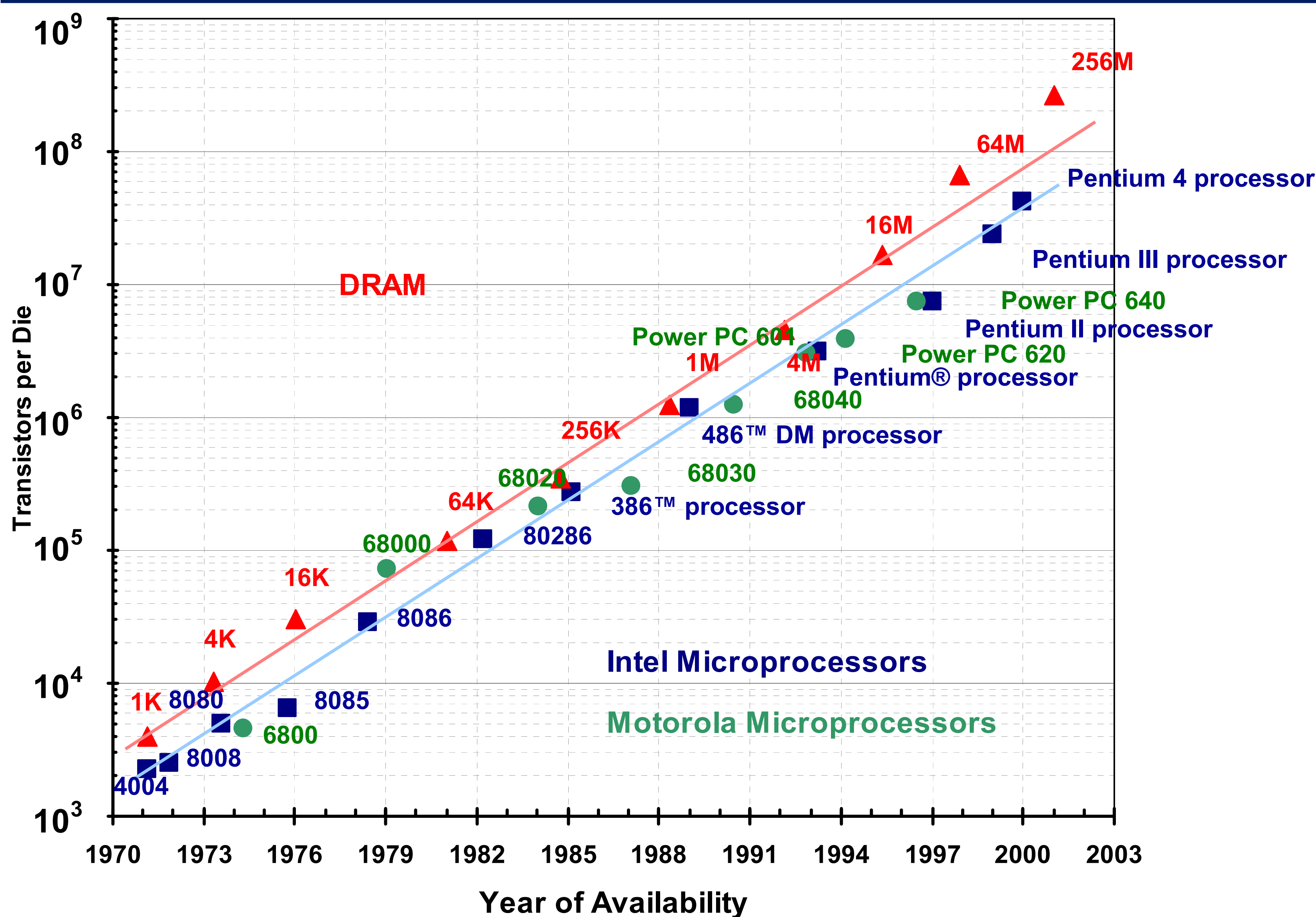
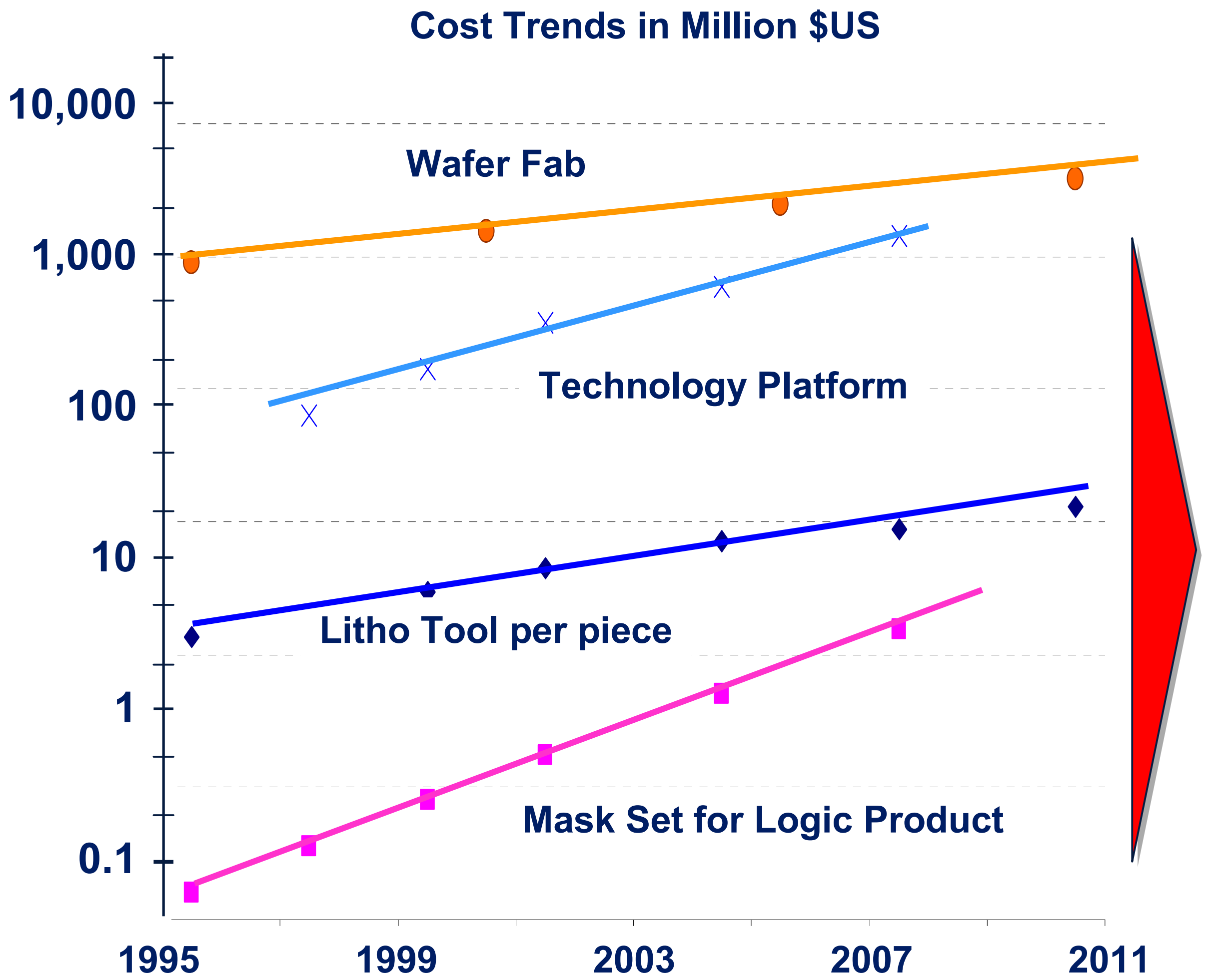
Moore‘s Law from 1970 to 2002, an exponential success story



But costs and invest also explodes exponentially!



Gordon E. Moore at the ISSCC 2003

NO EXPONENTIAL IS FOREVER . . .

Gordon E. Moore

Gordon E. Moore at the ISSCC 2003

NO EXPONENTIAL IS FOREVER . . .

BUT

WE CAN DELAY "FOREVER"

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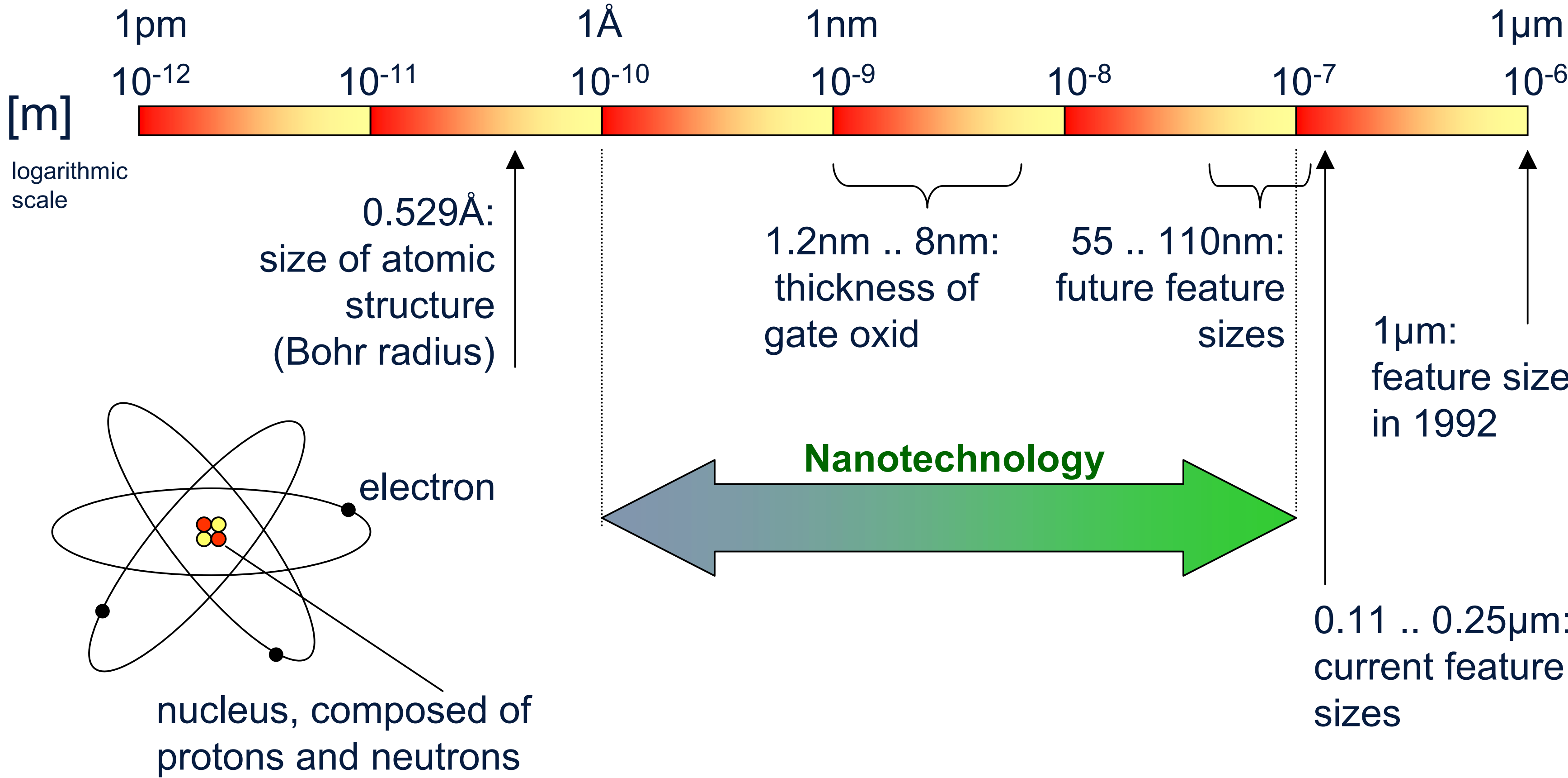
1 Micron and Below



1Å = 0.1nm = 10^{-10} m (Anders Jonas Ångström, 1814 - 1874)

Moore's Law and Scaling Theory

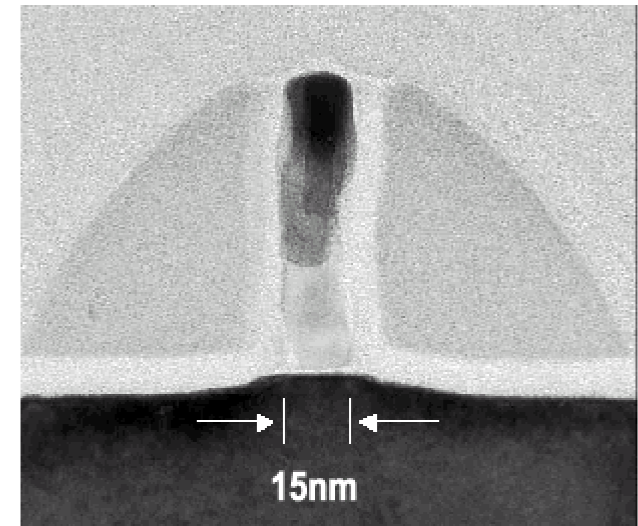
Scaling by a factor of α (about 1.4 every 2 years):

Voltage	V / α
Oxide thickness	t_{ox} / α
(Wire) width	W / α
(Gate) Length	L / α
(Junction) Depth	X_j / α
Substrate Doping	$N_A \alpha$

Results in

Density	$\approx \alpha^2$
Speed	$\approx \alpha$
Power per circuit	$\approx 1/ \alpha^2$
Power density	constant

Single-Gate FET



(AMD: IEDM 2001 late news paper)

Scaling Reality

With each technology generation we achieved:

- **Performance: 1.2x**
- **Density: 2x**
- **Power Consumption: 0.5x**
- **Cost: ≤ 1.15x**

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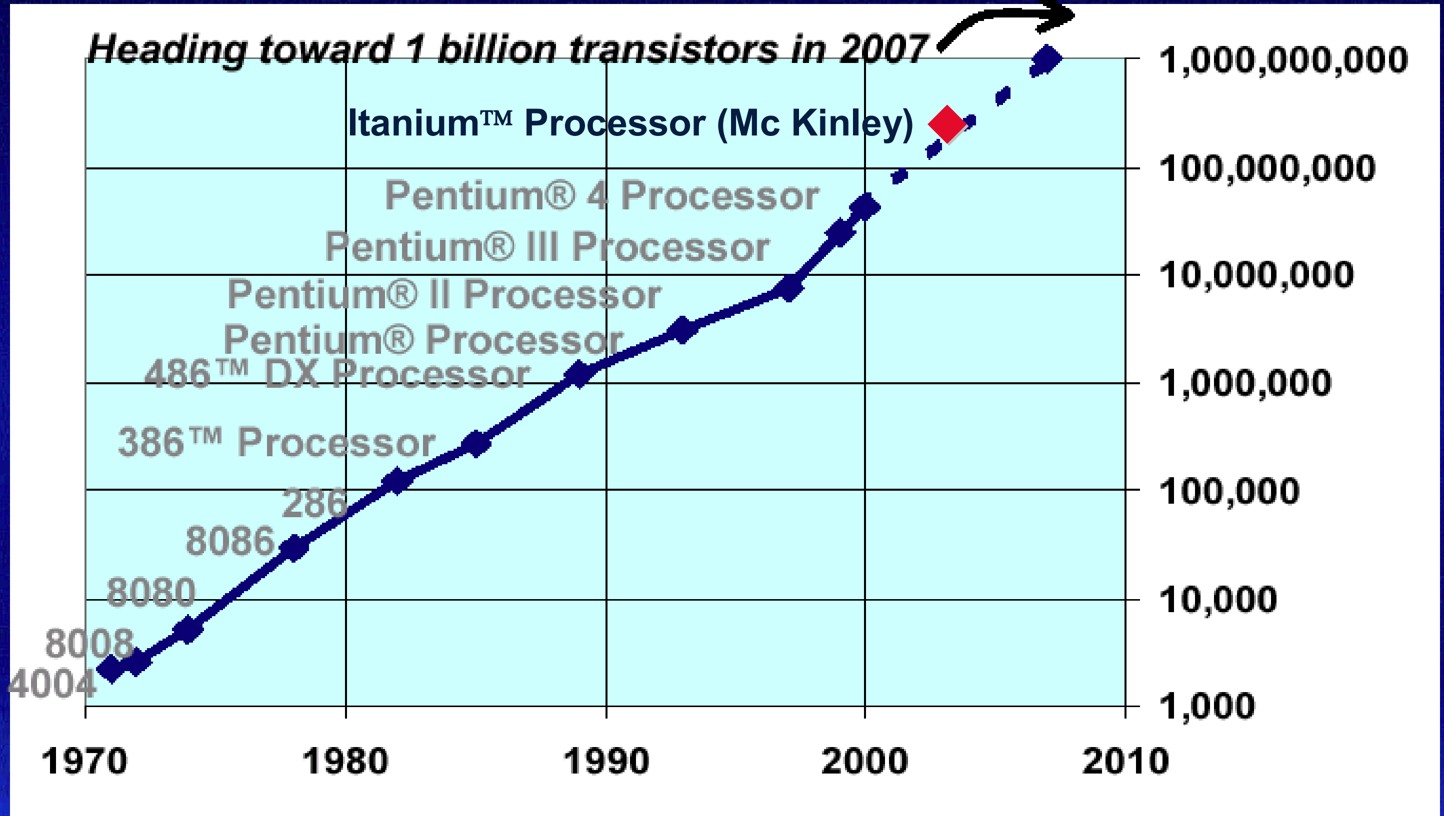
Technology Roadmap Devices



Lithography

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Technology Roadmap Lithography

Complexity increase

ASIC printed L_{Gate}	90nm	65nm	45nm	32nm	22nm
ASIC 1/2 Pitch	107nm	80nm	65nm	45nm	32nm
Year of Production	2003	2005	2007	2010	2013
Tool (λ) front-up / high Vol.	**193nm**	**193nm (HiNA)**	**157nm**	**EUV (13,4nm)**	**EUV (13,4nm)**
Tool (λ) altern. / low Vol.			*EPL/LEEPL, EBDW*	*EPL/LEEPL, EBDW*	*EPL/LEEPL, EBDW*
Mask Types	COG, HTPSM	COG, HTPSM, CPL / 3Tone	COG, HTPSM, CPL / 3Tone	Multilayer reflection Masks	Multilayer reflection Masks
Resist	single layer resist	bi-layer-resist, resist shrink process	bi-layer-resist, ultra-thin resist, hardmask	bi-layer resist	bi-layer resist
Enhancement	rule based and model based OPC, SRAF	model based OPC, SRAF	model based OPC, SRAF	OPC	OPC

Cost increase

Optical Litho

Next Generation Litho (NGL)

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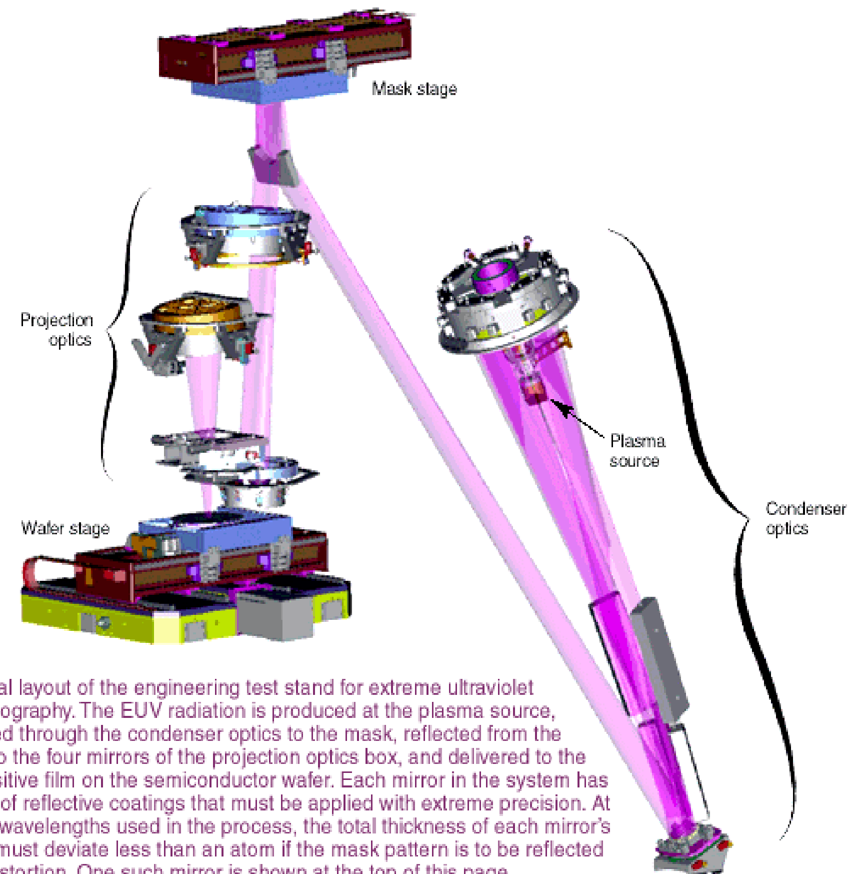
Technology Challenge - Litho Tool Costs
What is EUV lithography ?

- Shrink wavelength of exposure light:

  - 248nm manufacturing
  - 193nm development
  - 157nm pathfinding
  - 13nm/EUV research

- EUV light does not transmit through glass or air

-> EUV is a disruptive technology



The optical layout of the engineering test stand for extreme ultraviolet (EUV) lithography. The EUV radiation is produced at the plasma source, transmitted through the condenser optics to the mask, reflected from the mask onto the four mirrors of the projection optics box, and delivered to the EUV-sensitive film on the semiconductor wafer. Each mirror in the system has 81 layers of reflective coatings that must be applied with extreme precision. At the short wavelengths used in the process, the total thickness of each mirror's coatings must deviate less than an atom if the mask pattern is to be reflected without distortion. One such mirror is shown at the top of this page.

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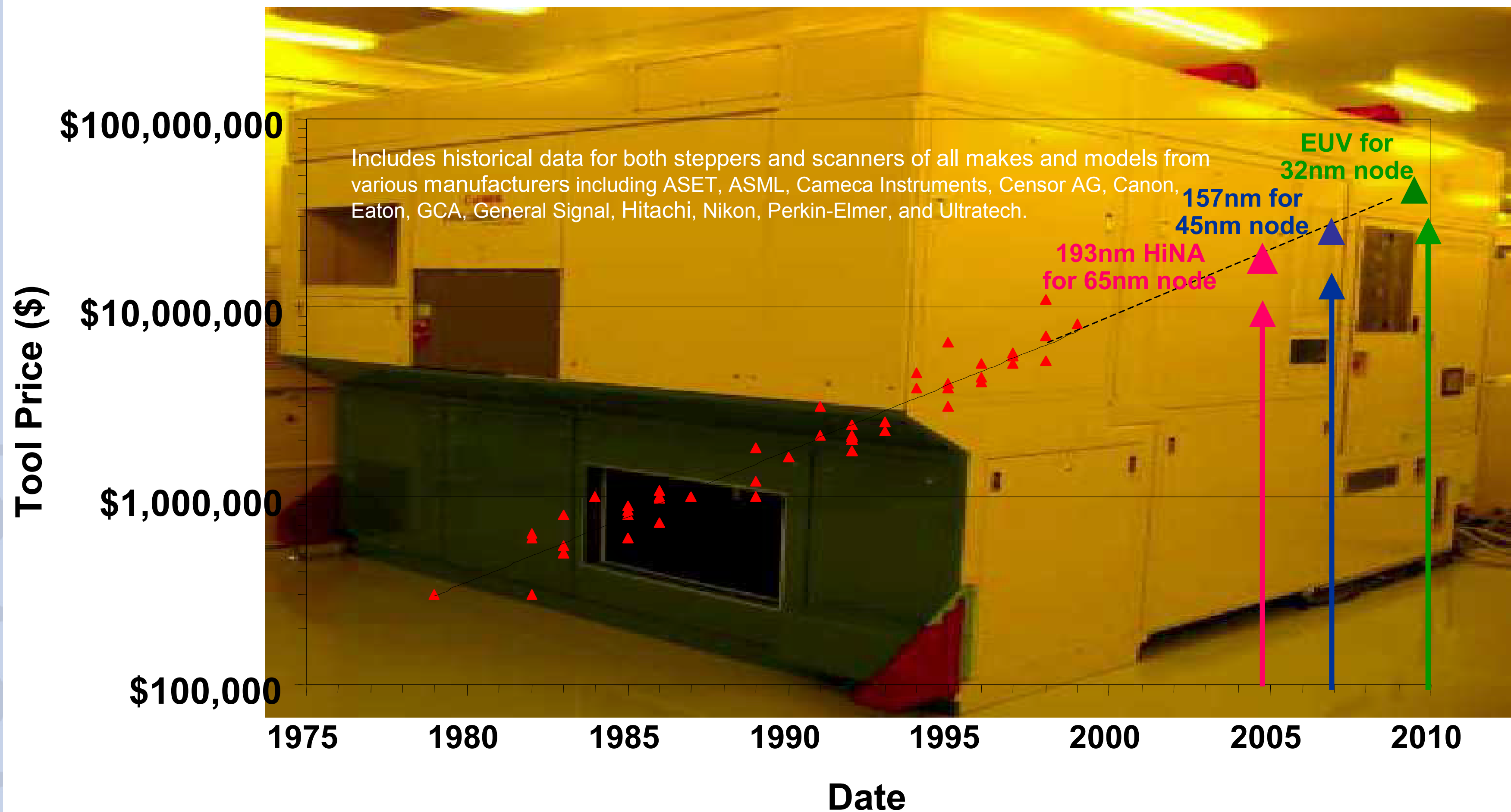
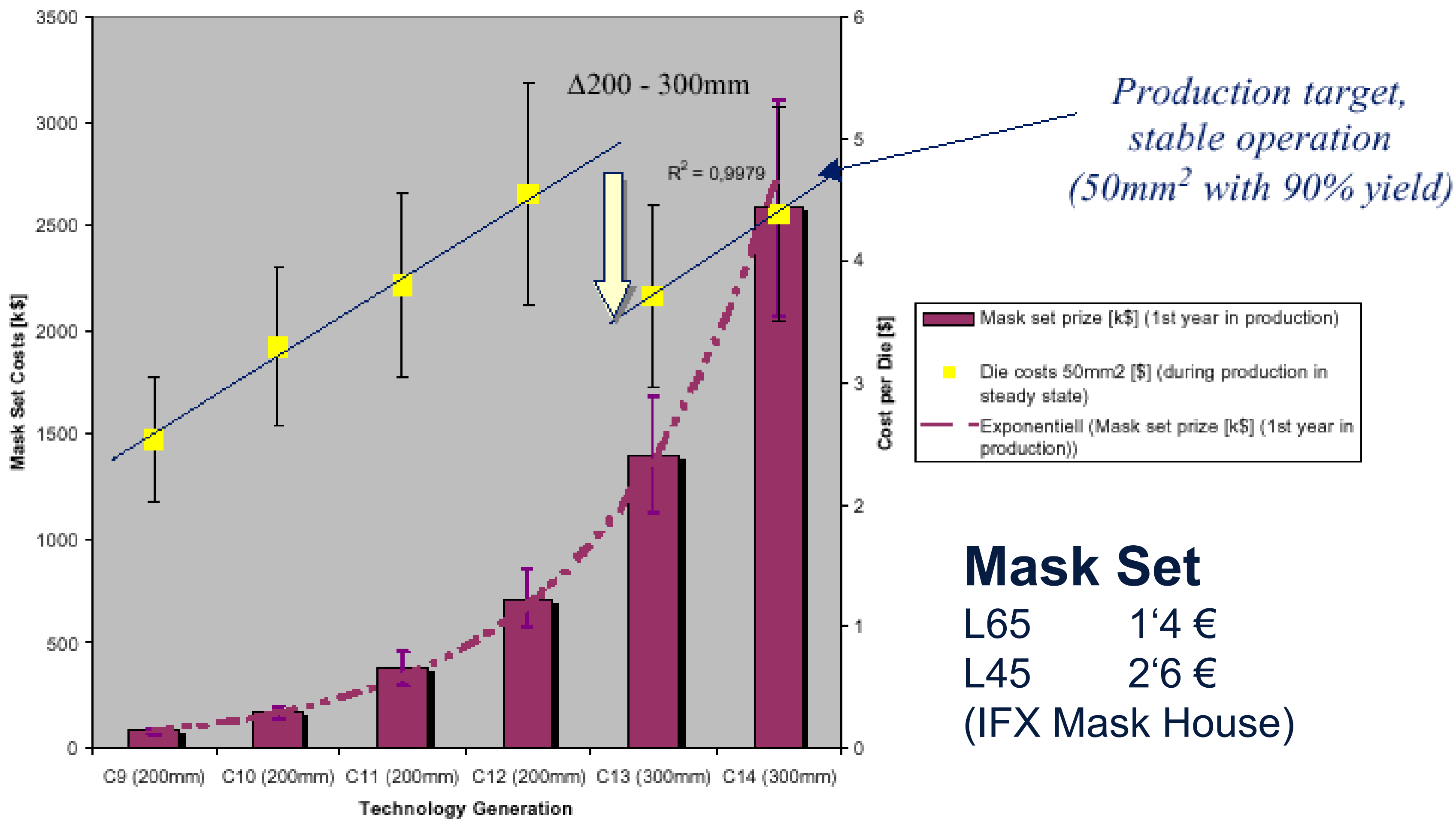
Technology Challenge - Litho Tool Costs
Is lithography still affordable ?



Background: CANON FPA-5800 FS1 - first world-wide 157nm pre-production tool

Technology Challenge - Mask Set & Die Cost

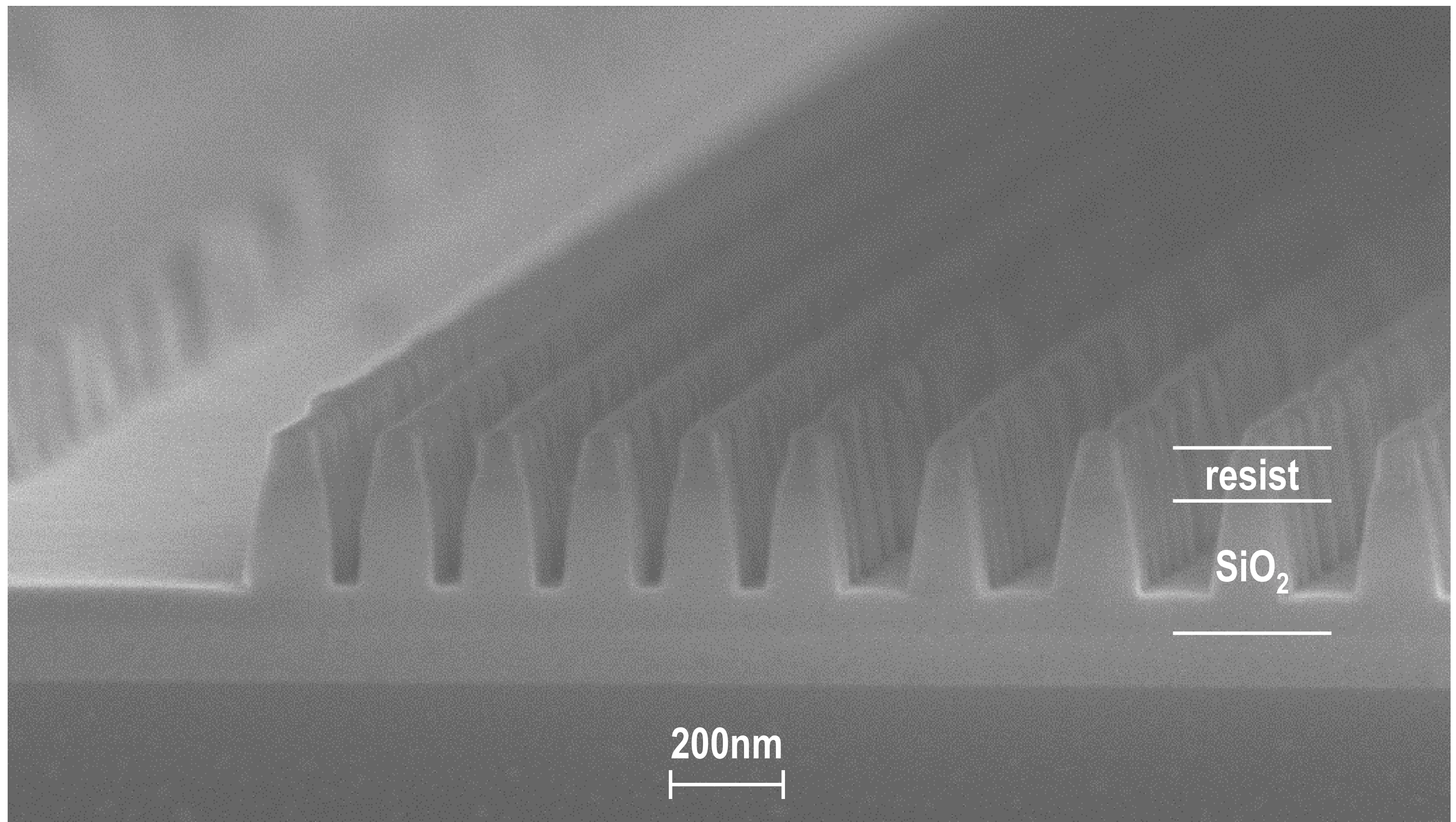


L65 L45

EUV Lithography - First Results

First Dielectric Etches with EUV Patterned Resist

IFX CPR NP: M. Engelhardt



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Low-k

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Technology Challenge - Metal Dielectric

Why low k?

Wiring Capacitance C_{wire} ~ **k** * L * f (h, w, d)

k - dielectric constant
L - wire length
h & w - wire height & width   d - distance to neighboring wires

Benefits of lowering k value:

+ Reduction of RC delay $RC \sim \rho * \mathbf{k} * L^2$

+ Reduction of power dissipation $P \sim C_{ges} V^2 f_c$
  - V - power supply voltage
  - f_c - clock frequency
  - C_{ges} - total capacitance: $C_{device} + C_{wire}$

+ Reduction of cross talk noise in hybrid scheme ($k_{metal} < k_{via}$) $V_x \sim C_{II} / C_{wire}$

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Technology Challenge - Metal Dielectric
Low k Inter- & Intrametal Dielectric Materials

- Si-Oxide (Si-O bonds) k ~ 4
- C-doped Oxide (CVD low k, Coral, BD) k ~ 2.9
- SOD organic polymers (SiLK, C-H bonds) k ~ 2.6
- Teflon (C-F bonds, ‘lowest bulk k‘) k ~ 2
- Vacuum / Air k ~ 1

k < 2 ===> Porous Dielectrics

„How to bring holes into Swiss Cheese ?“

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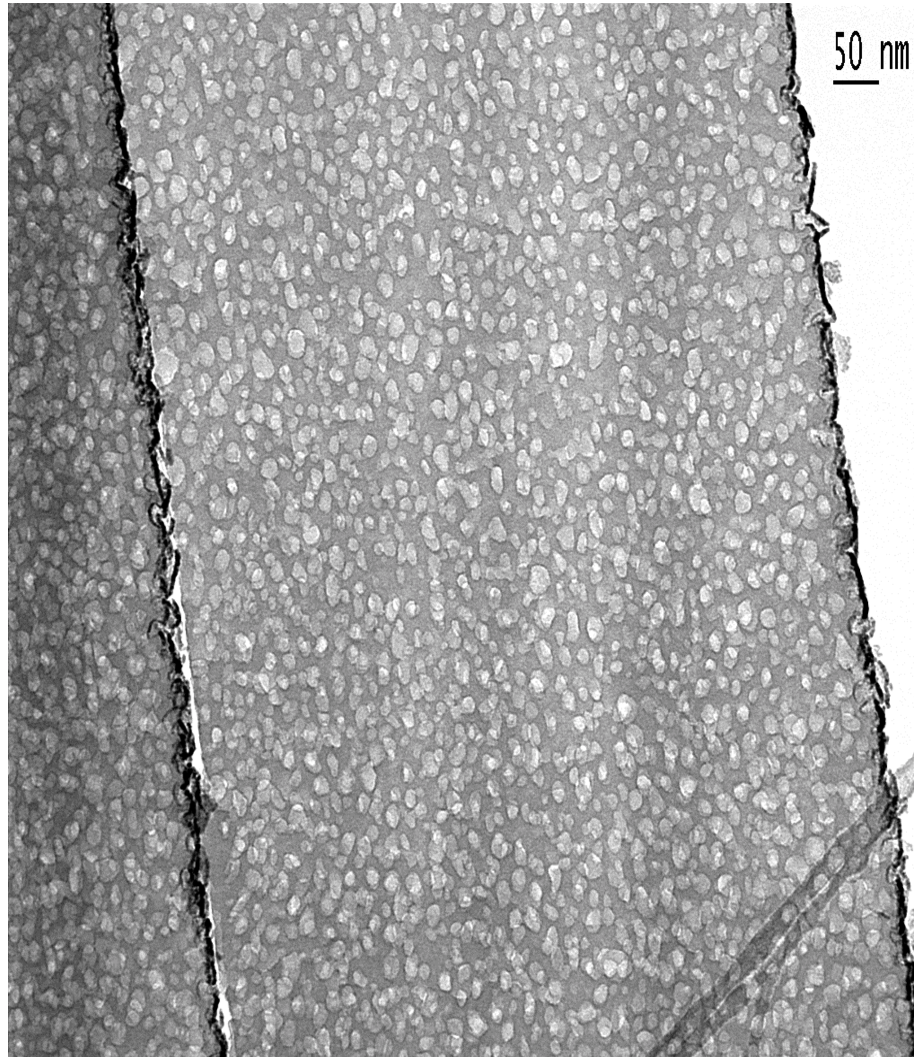
Technology Challenge - Metal Dielectric SiLK



Average Pore size ~ 16nm
Dielectric constant ~ 2.20
Modulus (GPa) ~ 2.7
Hardness (GPa) ~ .16

p-SiLK V8

Dow Chemical

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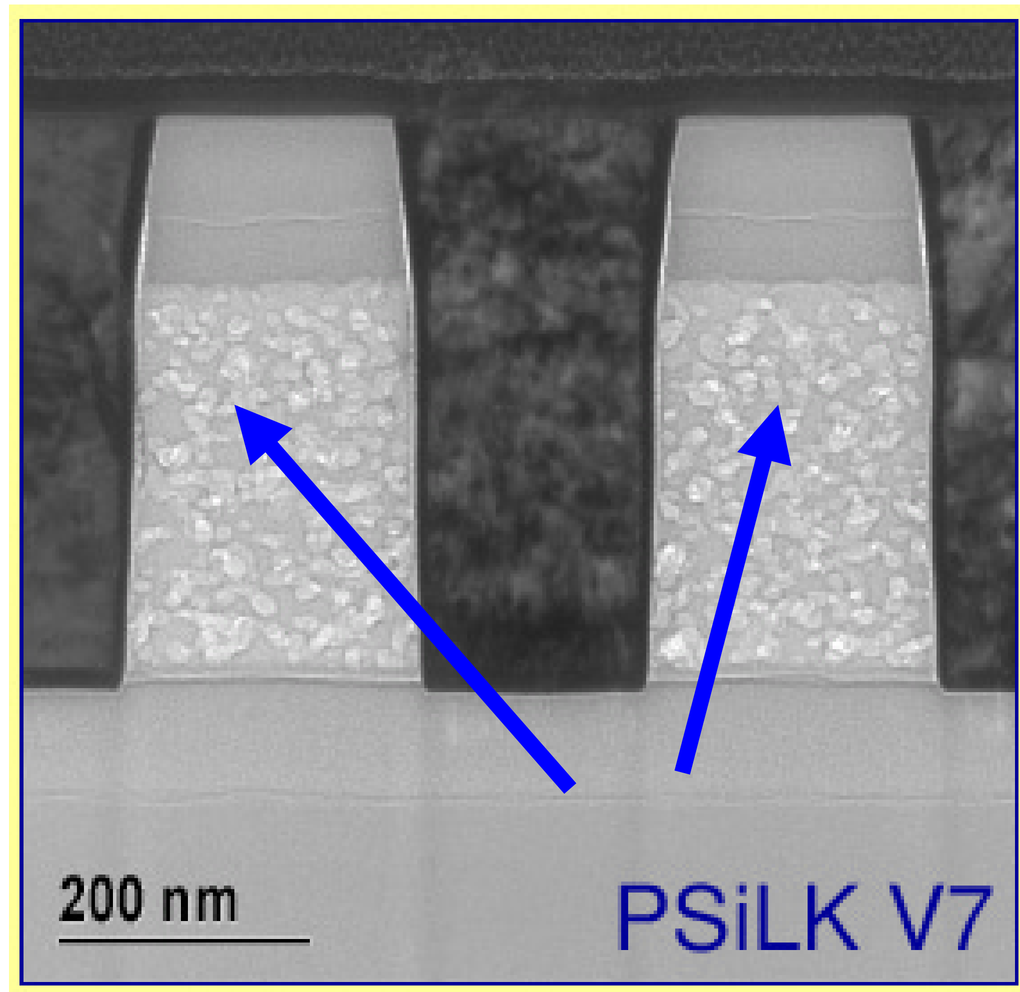
Technology Challenge - Metal Dielectric SiLK

Porous low k Integration

Average pore size

V7	25nm
Vfinal	< 10nm



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High-k

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Technology Challenge - Gate Dielectric

- Gate oxide today: only 5 (!) monolayers (16 Angström)
- 10 – 12 A needed for 65nm technology according to scaling theory
- but *tunneling current* through gate oxide exceeds ‘normal’ current!!
- ⇨ unacceptable high standby leakage (low power requirements!)
- gate dielectric materials with higher dielectric constant (then oxide) needed, which allow to further reduce the electrical layer thickness while increasing the physical one (which reduces gate tunneling current)
- high k materials urgently needed for further device scaling

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Technology Challenge - Gate Dielectric
Potential High k Gate Dielectric Materials

Reference
SiO_2 3.9

Material	k	Material	k
Al_2O_3	**8-11.5**	$NdAlO_3$	22.5
$Al_xSi_yO_z$		$PrAlO_3$	25
$(Ba,Sr)TiO_3$	200-300	**Si_3N_4**	**7**
$BeAl_2O_4$	8.3-9.43	$SmAlO_3$	19
CeO_2	16.6-26	**$SrTiO_3$**	**150-250**
$CeHfO_4$	10-20	**Ta_2O_5**	**25-45**
$CoTiO_3/Si_3N_4$		Ta_2O_5-TiO_2	
$EuAlO_3$	22.5	**TiO_2**	**86-95**
HfO_2	**26-30**	TiO_2/Si_3N_4	
Hf silicate	**11**	**Y_2O_3**	**8-11.6**
La_2O_3	**20.8**	$Y_xSi_yO_z$	
$LaAlO_3$	23.8-27	**ZrO_2**	**22.2-28**
$LaScO_3$	30	**Zr-Al-O**	
La_2SiO_5		**Zr silicate**	**11-12.6**
$MgAl_2O_4$	8.3-9.4	$(Zr,Sn)TiO_4$	40-60

**C.A. Billmann et al, MRS Spring Symposium, 1999, *R.D. Shannon, J. Appl. Phys. 73, 348, 1993*

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Technology Challenge - Gate Dielectric

High k Gate Dielectric - Technical Issues

Integration with Si (or dual metal) gate

B Blocking (w/Poly)

Integration / Fab Contamination

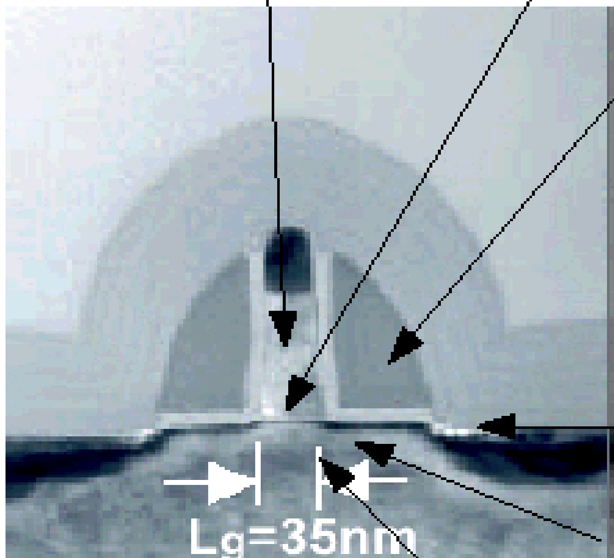
Leakage << SiO_2

Composition Control/ Phase Separation

Etch Properties

Reliability

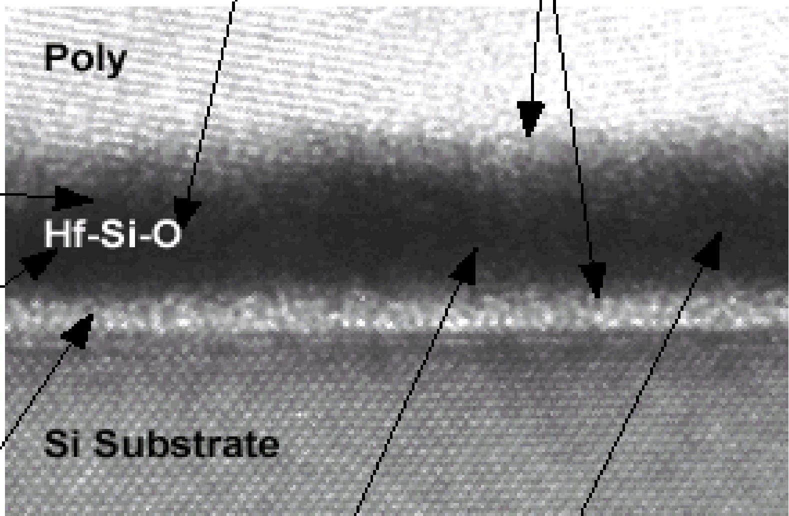
Channel Mobility



AMD 35nm Tranisitor (O/N dielectric)
VLSI 2001 Tech. Digest p.9

Material Selection

Interface Reactions



AMAT Hf-Silicate w/Poly

O2 Diffusion

Thermal Stability

EOT Scaling

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Technology Challenge - Gate Dielectric

High k Gate Dielectrics: Status & Major Issues today

- best reproducible thicknesses today 12A EOT (21A Tox_inv), >> HfSiON << e.g. TI, AMD
- leakage goal realized in few isolated cases with significant drawbacks for mobility, Vt-shift, and reliability
- mobilities around 30 - 80%, depending on field & measurement conditions and techniques
- Vt adjustment not possible yet (esp. for pFET) due to traps & charges
- dielectric reliability is major issue
- high k dry/wet etching in development
- integration scheme for triple gate oxide not finalized

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Future Technologies

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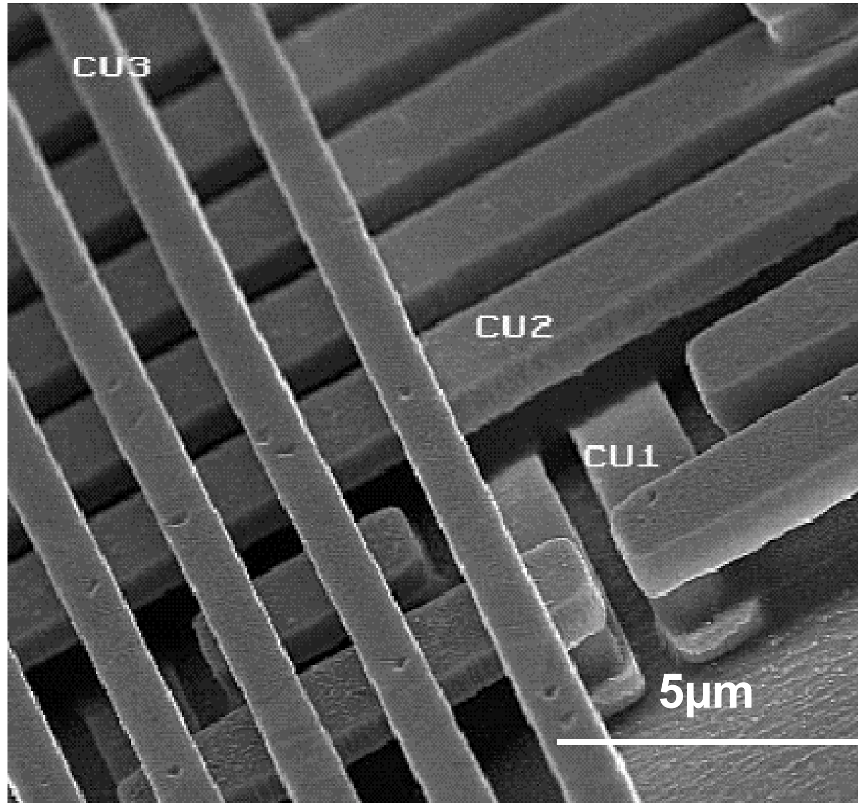
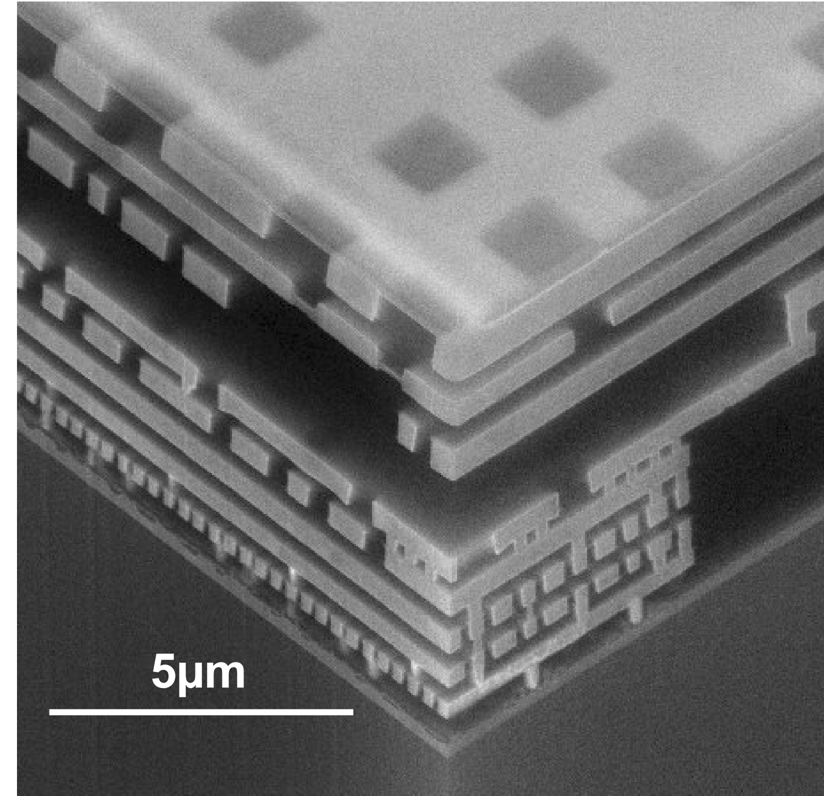
Interconnects: Yesterday and Today



Yesterday: 350nm, 3 Layers



Today: 130nm, 10 Layers

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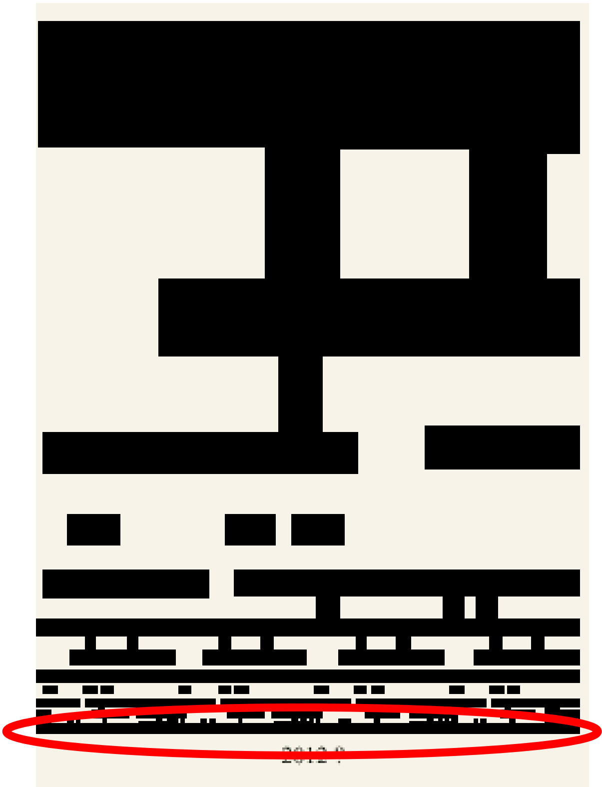
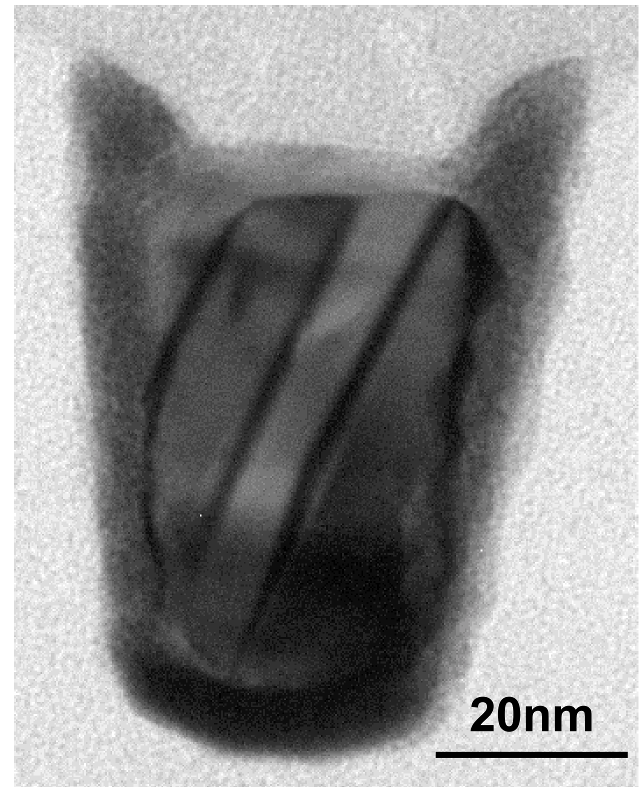
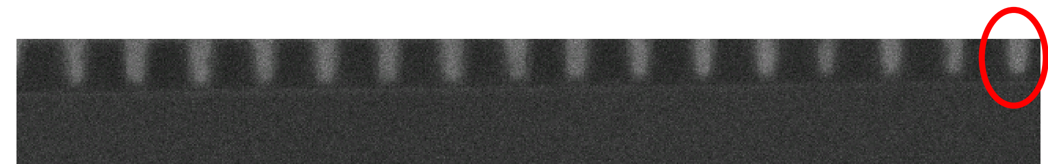
Interconnects: Tomorrow



Source: IBM



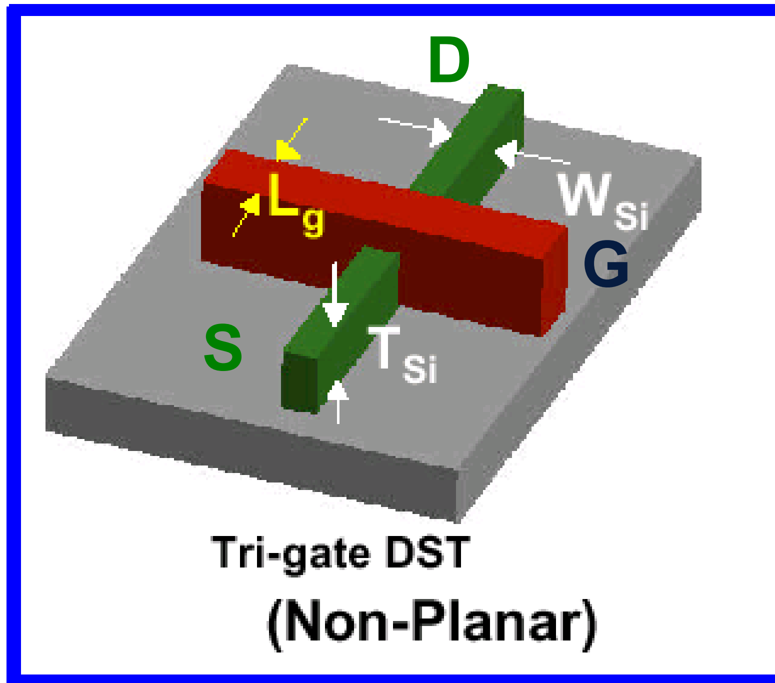
Source: Infineon, CD=35nm

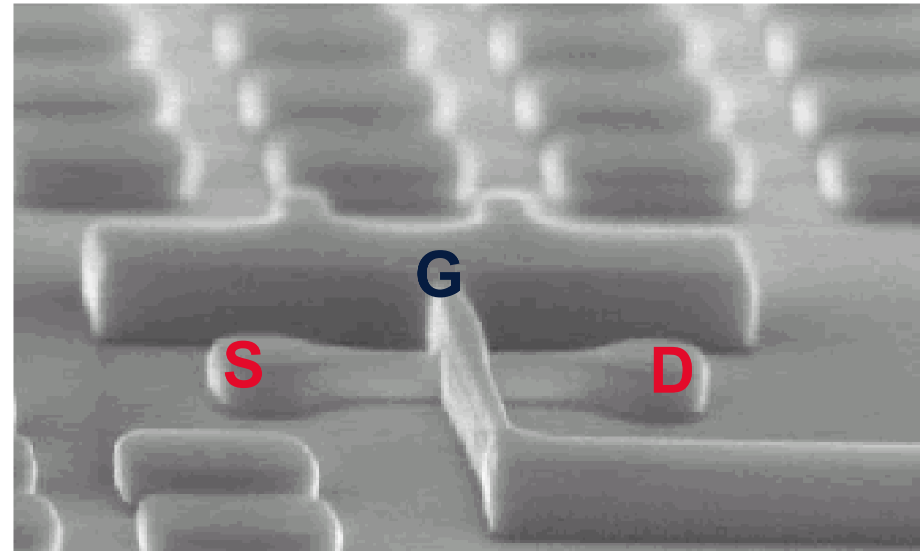


Source: Infineon, CD=70nm

Technology Challenge - Device Off Current

Novel Devices: Example Tri-Gate - SOI





- Three gates control an ultrathin Si film -> improved SCE
- Opens scaling opportunity down to Lg ~ 10nm
- **BUT very difficult to integrate**

[R. Chau, Intel, SSDM 2002]

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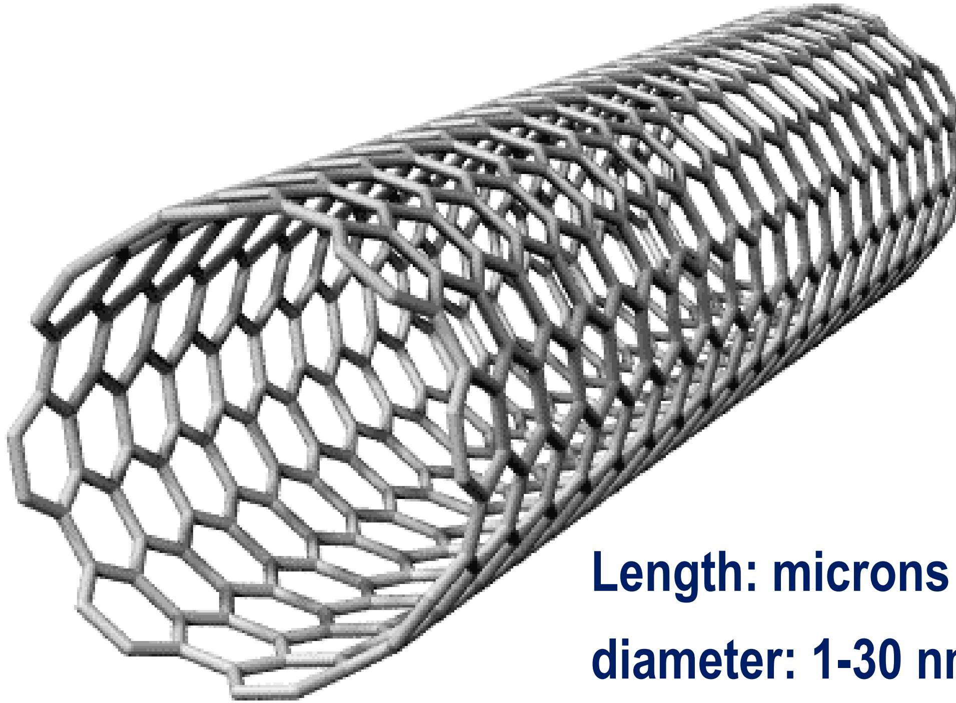
Carbon Nanotubes:
Extending Moore´s Law Beyond the End of the Roadmap



Length: microns - millimeters

diameter: 1-30 nm

electrical conductivity: metallic or semiconducting

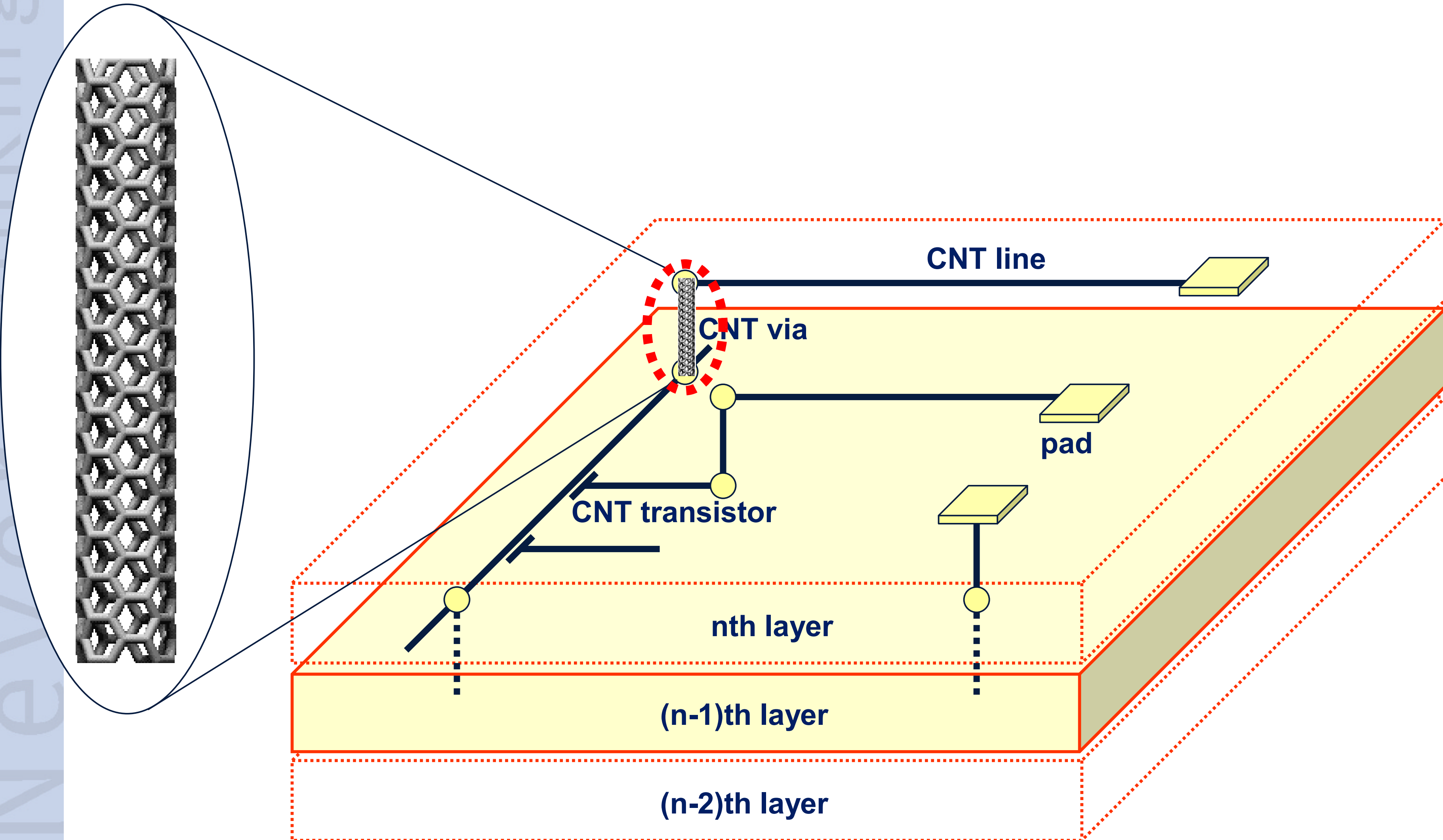
ballistic electron transport

current density: 10^{9} A/cm^{2}

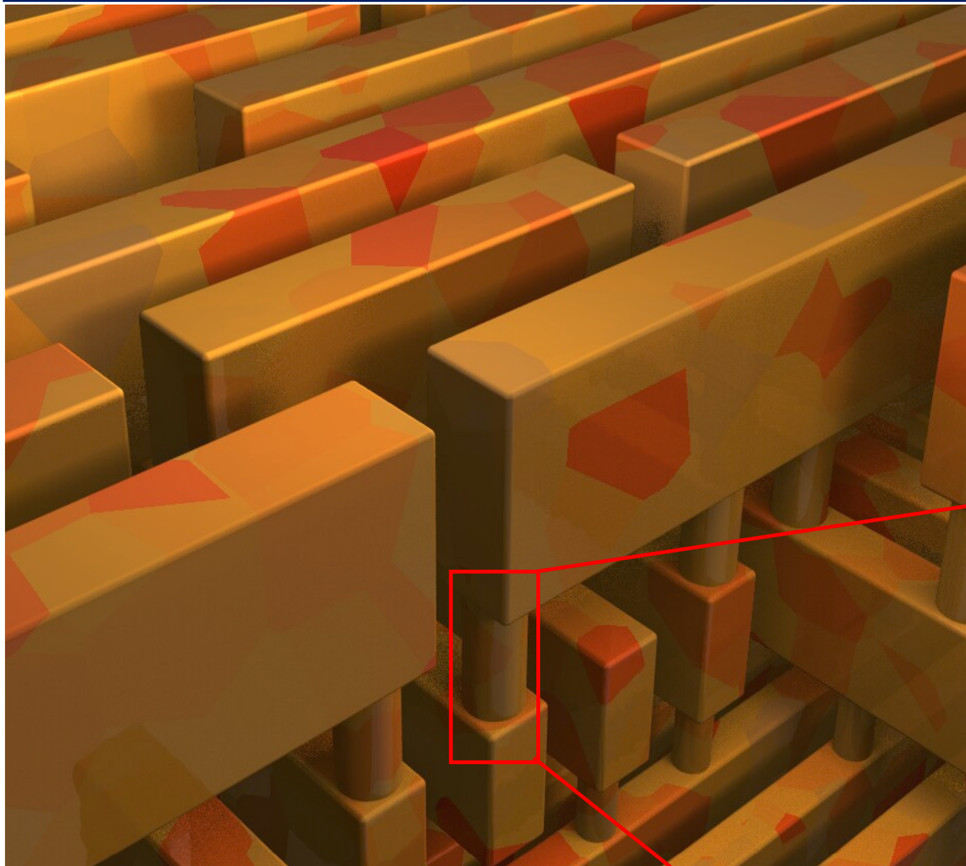
e-modulus: 1000 Gpa → elastic elongation of 40%

thermal conductivity: >3000W/m/K

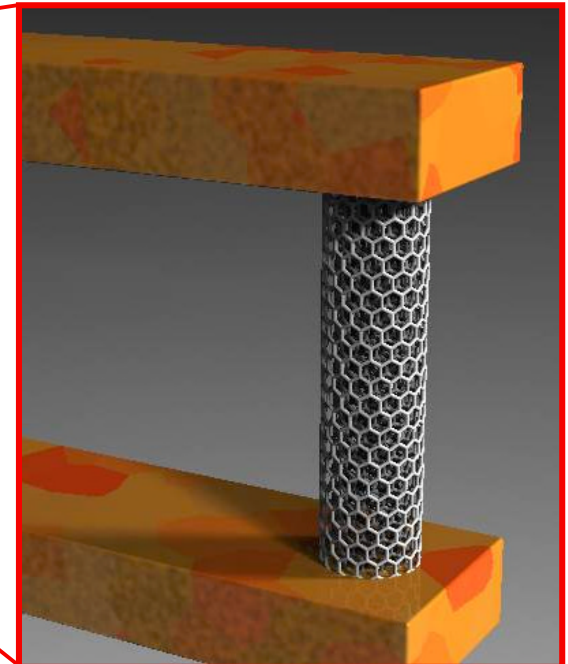
Carbon Nanotubes: Electronic Devices and Wiring



Carbon Nanotubes: Vertical Interconnects



Via Fill with CNT



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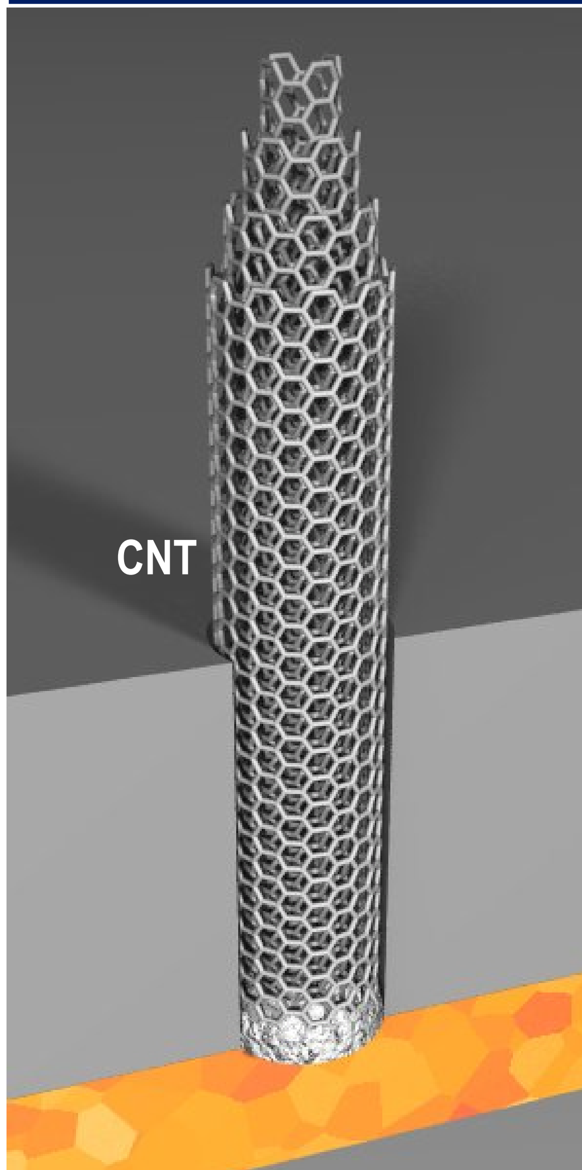
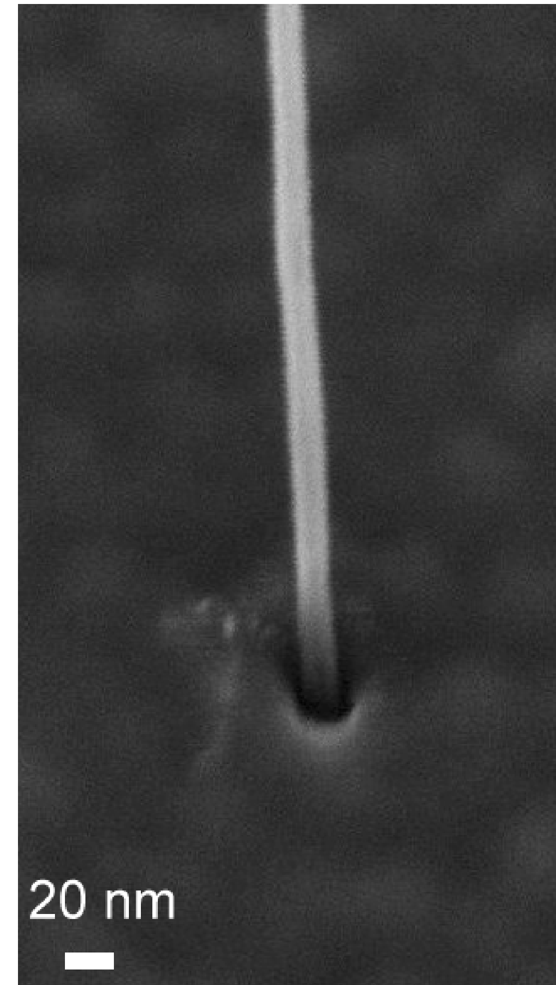


Via filled with CNT ($Ø_{via}$≈35nm)



Source: G. S. Düsberg, A. P. Graham, M. Liebau, R. Seidel, E. Unger, F. Kreupl, W. Hönlein, Nano Lett. 2003, 3, 257-239

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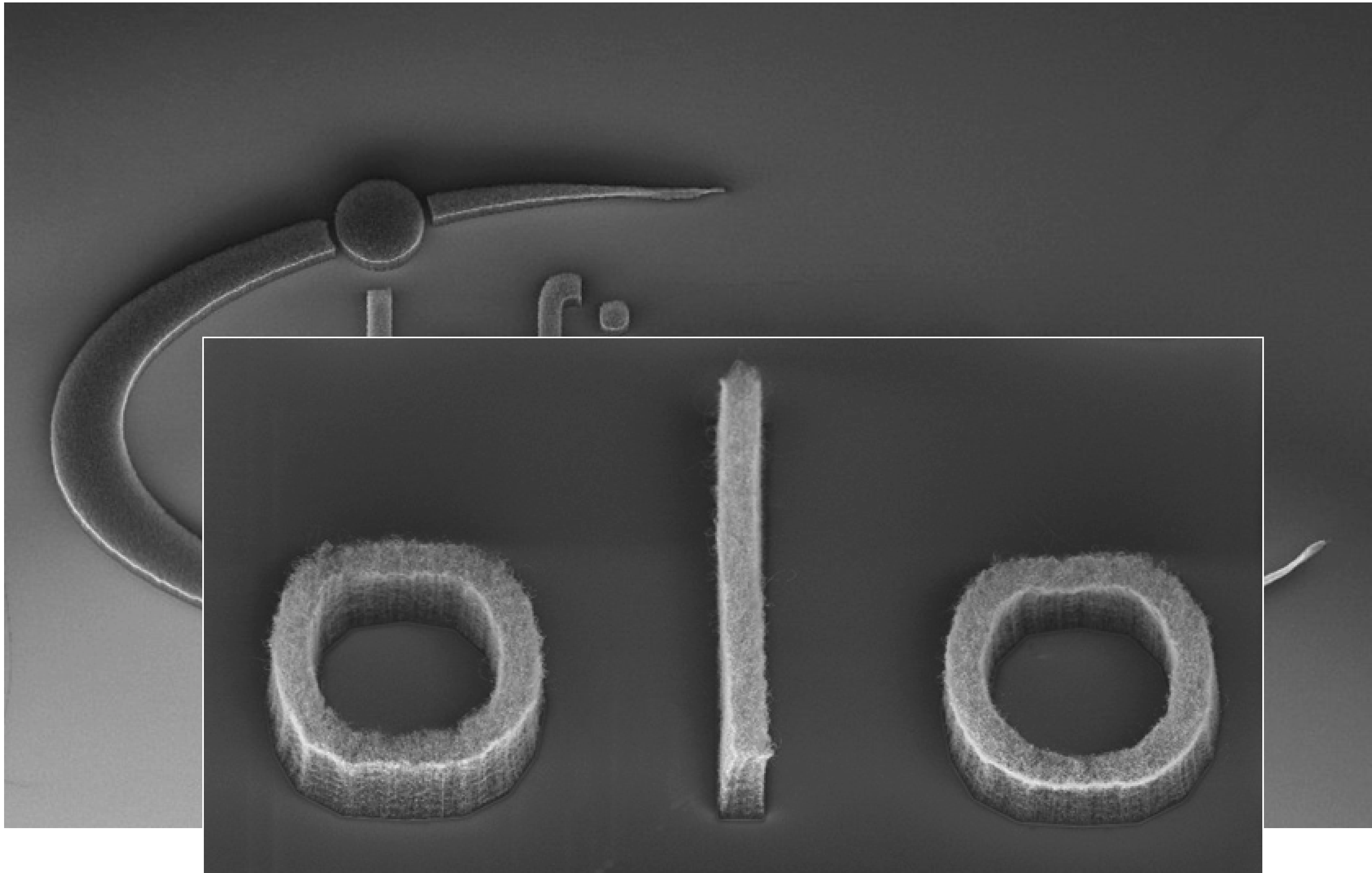
Carbon Nanotube Logo



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Biochips

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Infineon's activities in the biochip sector

Optical biochips

- Flow-Thru-Chip: Based on specially developed silicon process
- Used in drug development
- Partnership with Metrigenix
- Products available

Electronic biochips

- Fully electronic DNA-chip: Integrated analysis electronics
- To make medical diagnosis in hospitals and in medical practices less costly, faster and more efficient
- Partnerships from Sibanat project
- First prototypes available (announcement in March 2002)

Neuro-Chips

- Neuro-Chip: Measurement of electrical activity of living cells
- Scientific cooperation with Max Planck Institute, Martinsried, Germany
- First demonstrator available (announcement in February 2003)

Share in startup companies in the biochip sector

- Advalytix (Germany), Metrigenix (USA), Febit (Germany)

Applications for biochips

- **Today**
  Biochips accelerate the selective development of medicines (development of new drug substances in large pharmaceutical laboratories).

- **Medium-term**
  Biochips can make medical diagnosis in hospitals and in medical practices cheaper, faster and more efficient.

- **Long-term**
  Biochips will permit personalized, individual medication.

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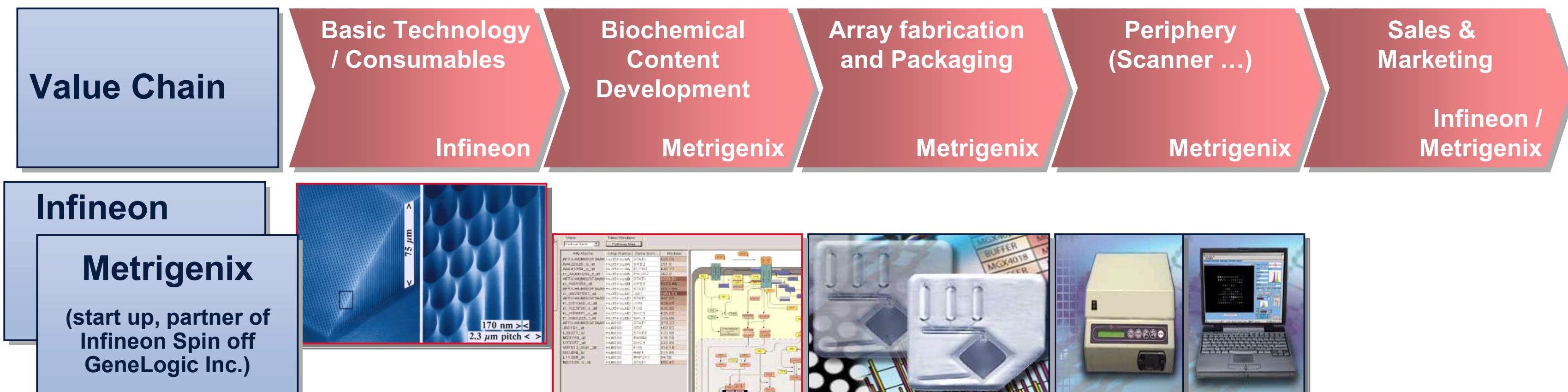
Optical Flow-Through

Optical biochips
System solution for drug development and diagnostics

- Through a partnership with Metrigenix Inc., a biochip system solution has been established.
- The system includes biochips with defined or customized content, hybridisation unit, detection unit and analysis software.
- Biochip is based on Infineons' porous silicon.
- First applications are in the field of drug development, further developments will permit diagnosis and individual medication.



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Optical biochips based on Infineons' porous silicon

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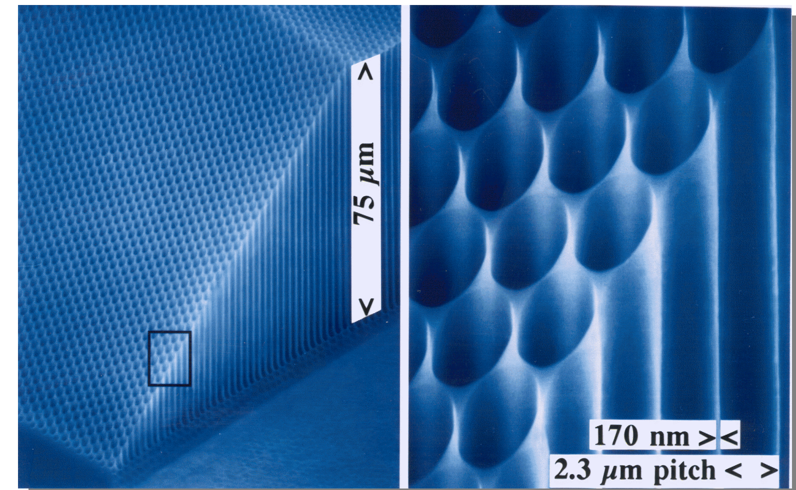
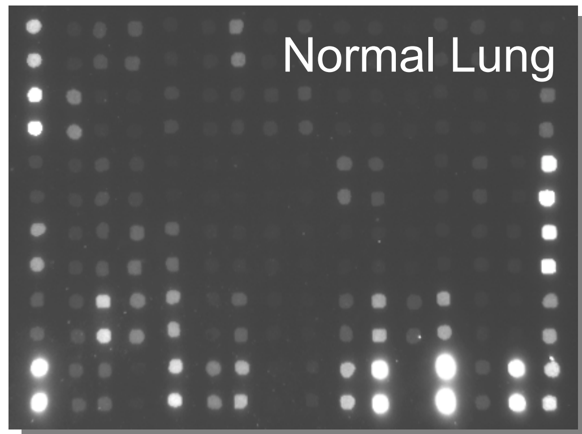
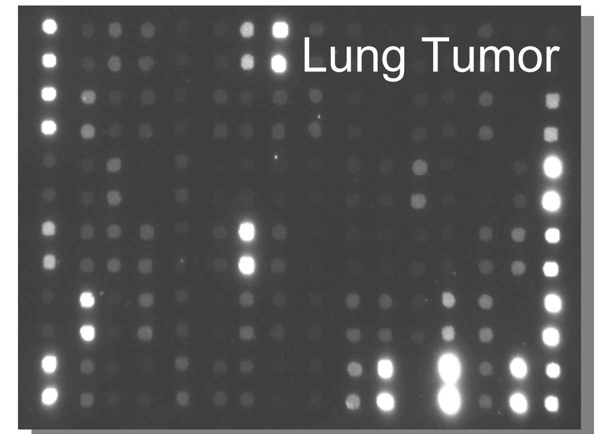
- Substrate is fabricated using an electrochemical etch process compatible with Infineon's semiconductor processes and mass production capabilities.
- Microstructured pores have a diameter of 10 µm, that is a tenth of a human hair.
- 1 Million pores on one square centimeter.
- Oligonucleotides are attached to the walls of the channels. As a result we have a very high surface area which contributes to the sensitivity and robustness of our solution.
- Reagents are pumped through the pores (flow-thru technology) accelerating analysis time.



Optical biochips
Application in drug development and diagnostics

- The flow-thru chip will accelerate the drug development process. Chip technologies have the potential to shorten the development time for new drugs of 12-15 years by 1-2 years.
- First applications are in the field of oncology (e.g. lung cancer, breast cancer), inflammation and neural degeneration (e.g. Alzheimer).
- The flow-thru chip will be further developed to accelerate diagnosis (e.g. differentiation of cancer subtypes) and to permit for individualized medication.





Electronic DNA-Chip

Infineon technologies
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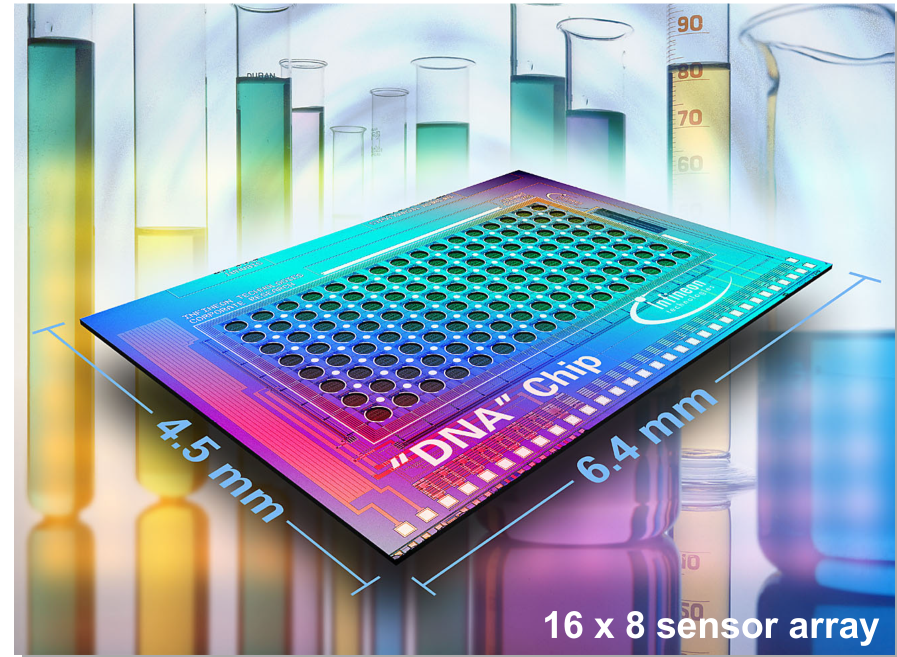
Fully electronic DNA-chip
First Biochip with integrated electronics

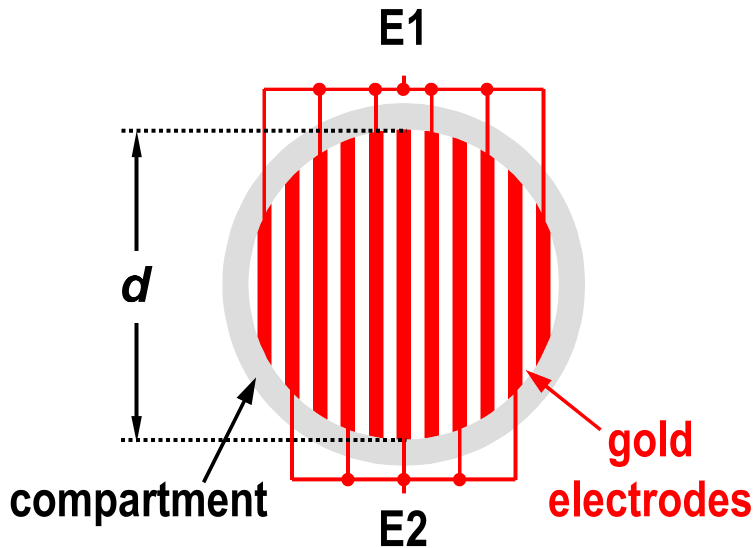
Why fully electronic DNA-detection



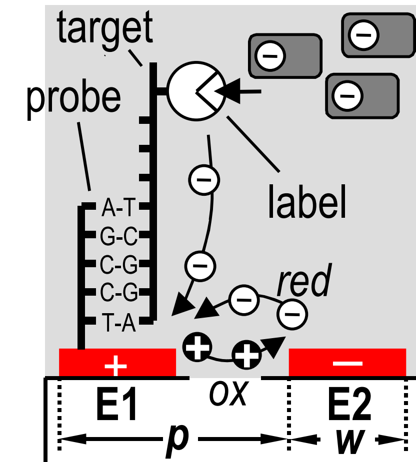
- Robust & easy operation of electrical systems
- Optical components are completely avoided and replaced by inexpensive electrical components
- Access to new fields of application, new markets (e.g. diagnosis in hospitals and doctors' offices)

Fully electronic DNA-chip
Detection principle

Top view of sensor / transducer



Cross section and current generation process



Typical dimensions: d = 100 ... 250 µm, w = 1 µm, p = 1 µm

Nucleotides are attached to the Au electrodes on a passivated CMOS surface.
Matching of labeled DNA changes enables an electrochemical redox reaction.
Signal processing is used to extract the biological information.

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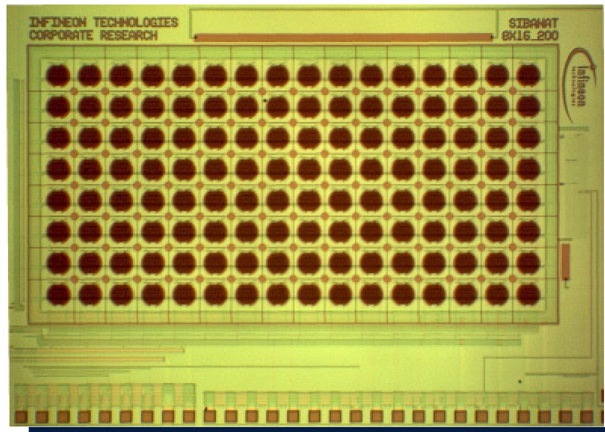
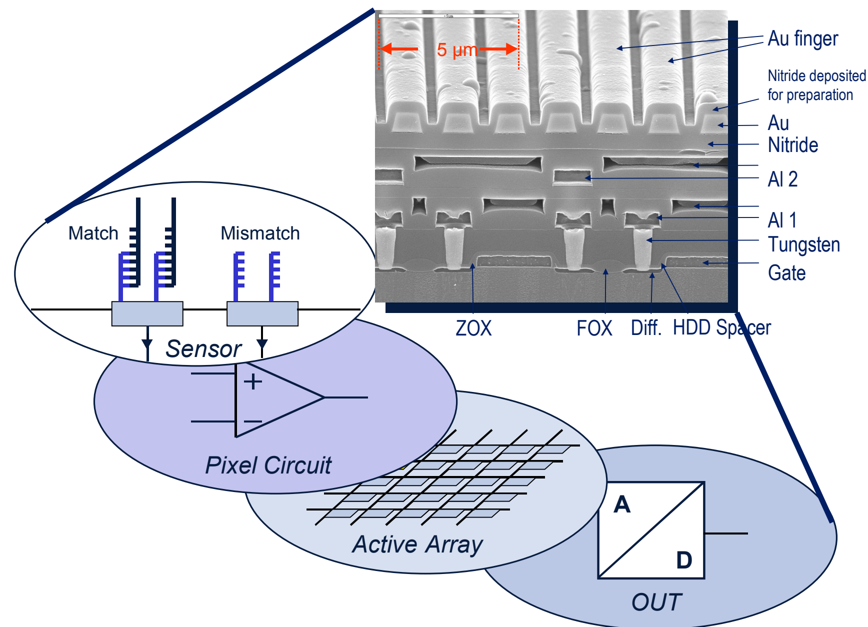
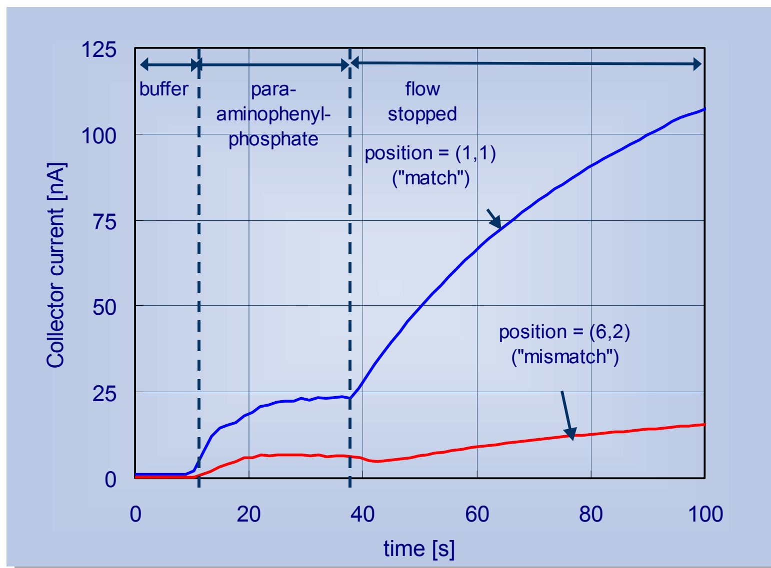
Fully electronic DNA-chip
Initial results



Chip photo: Fully electronic 16 x 8 sensor array

Technology cross section





Experiments with biological material reveal successful electronic DNA detection.

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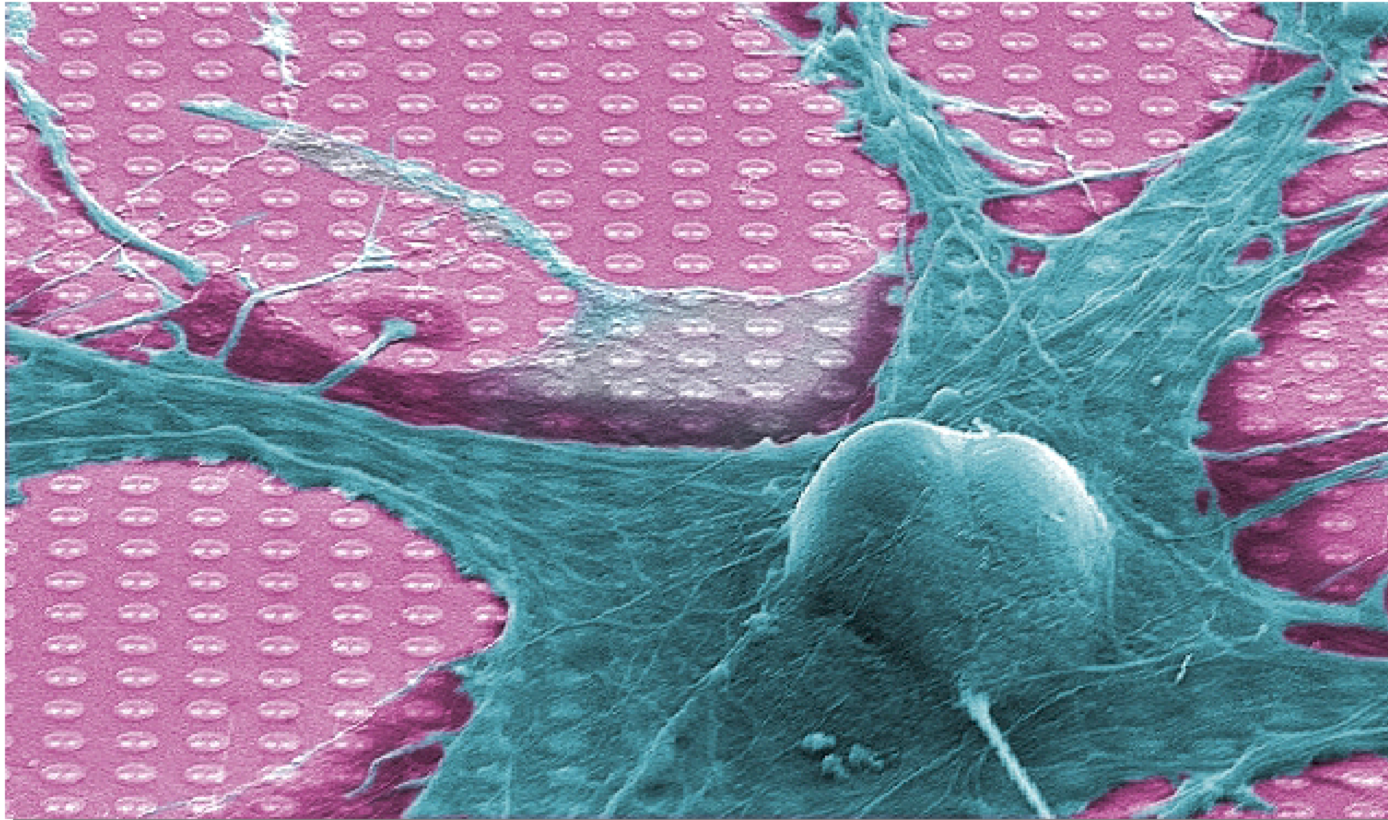
Neuro Chip

Sönke Mehrgardt
Oldenburg

Neuro-Chip
Infineon's chip for neurobiology and drug discovery

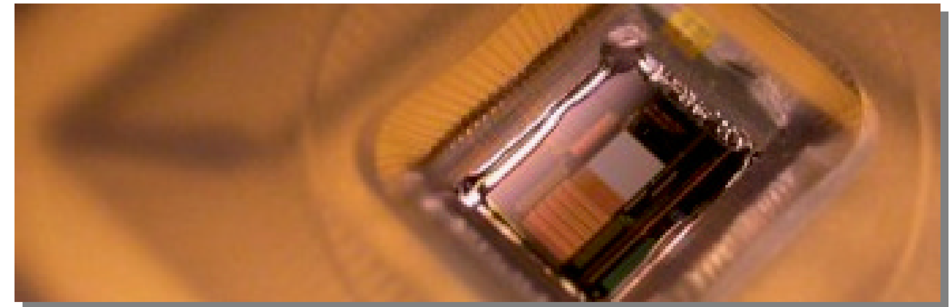
- Non-invasive long-term recording of nerve cells
- Applications in neurobiology and drug discovery



Snail cell grown on the biocompatible surface of the Neuro-Chip

Neuro-Chip
Chip properties

- The chip holds 128 × 128 sensors in an area of 1 × 1mm².
- Infineon has extended a standard CMOS-process by a biocompatible surface layer.

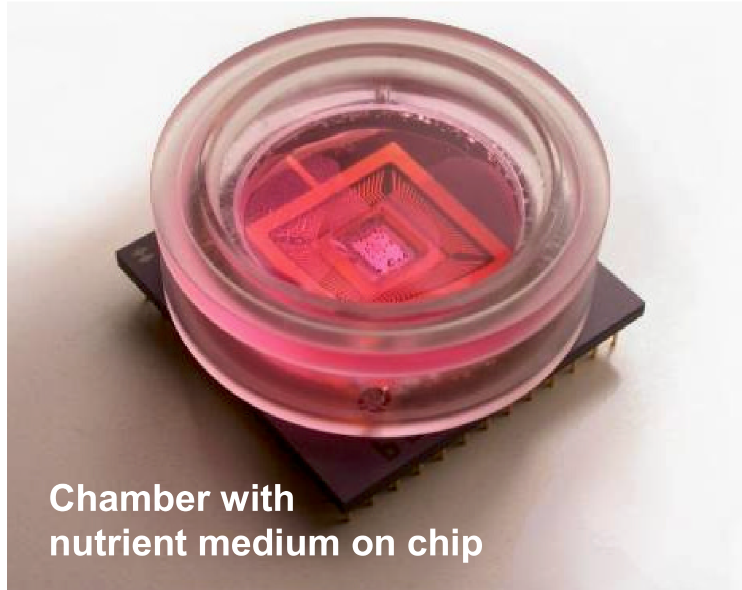


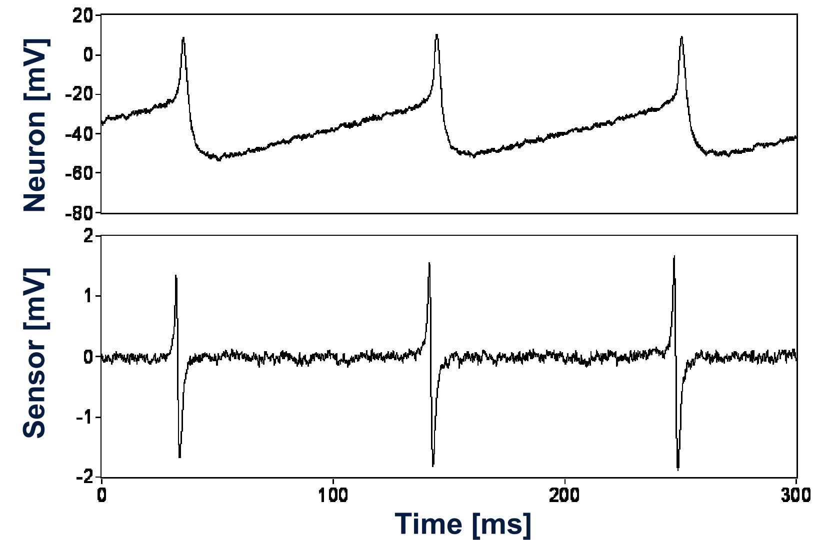
Sensor area (grey) and on-chip preamplifier (brown)

- Each sensor contains an electronic circuit with a unique self-calibration mechanism, a key technique for high-density sensor integration.
- The sensor's non-invasive recording method maintains the viability of the biological tissue over a long period of time.

Neuro-Chip
Successful biological measurements

- Infineon has been collaborating since mid-2000 with researchers at the Max-Plank-Institute for Biochemistry in Martinsried (Munich).





- In the field of neurological drug development, the Neuro-Chip will enable tests of the effects of new pharmaceuticals on living neurons.

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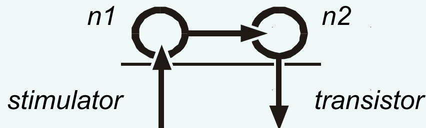
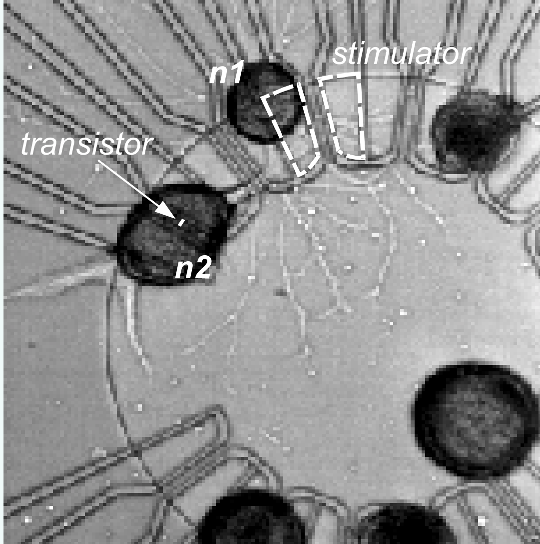
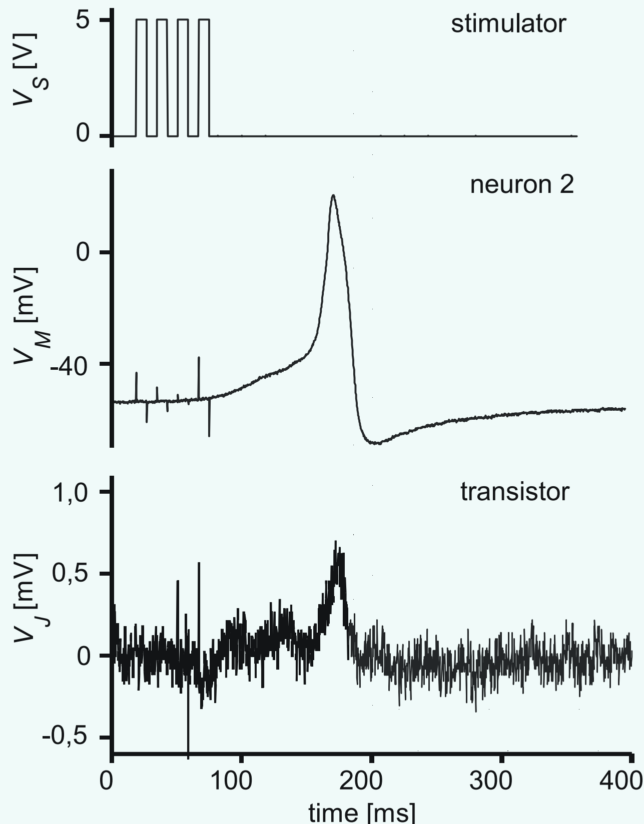
Basic Bio-Electronic Loop

Electronic Stimulation → Synaptic Transmission → Electronic Recording







Max-Planck-Institute for Biochemistry, Munich

M. Jenkner, P. Fromherz, *Interfacing a Silicon Chip to Pairs of Snail Neurons connected by Electrical Synapses* Biol.Cybernetics 84, 239-249 (2001)

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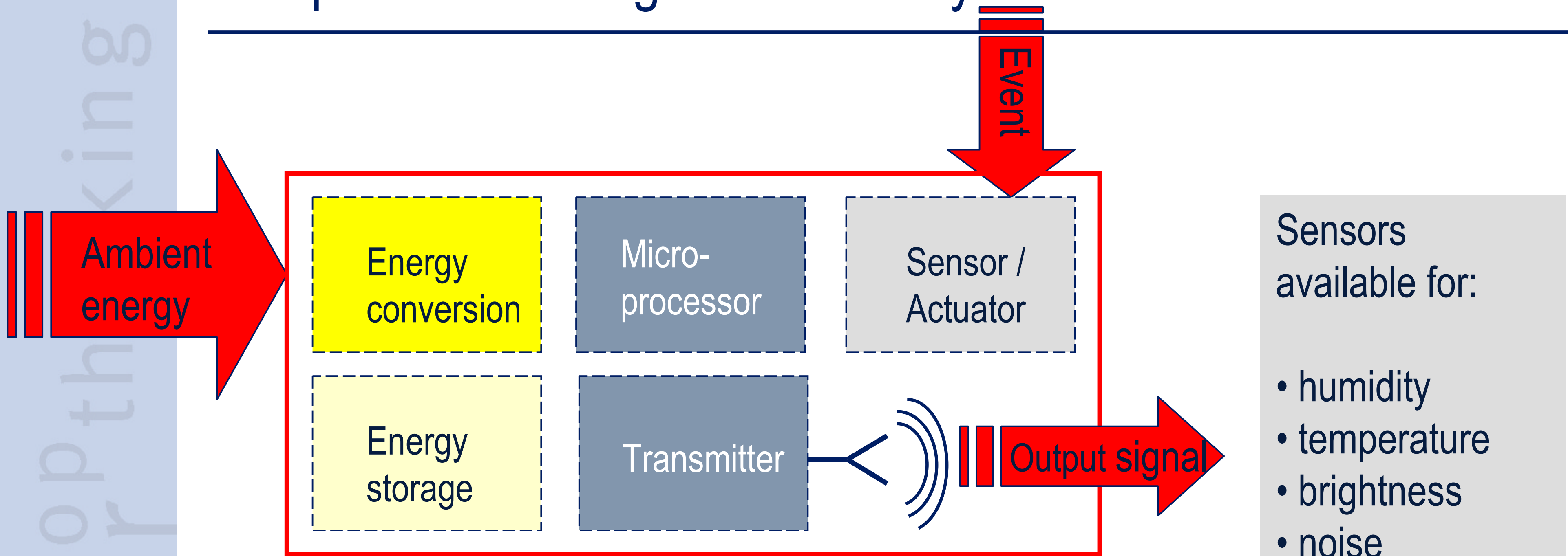
Power Supply

Self-powered Intelligent Sensor Systems



Sensors available for:

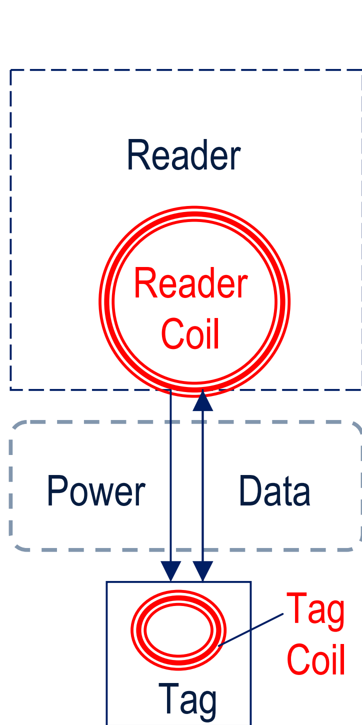
- humidity
- temperature
- brightness
- noise
- gas / smoke
- acceleration
- motion/vibration
- ....

Advantages of self-powered sensor systems:

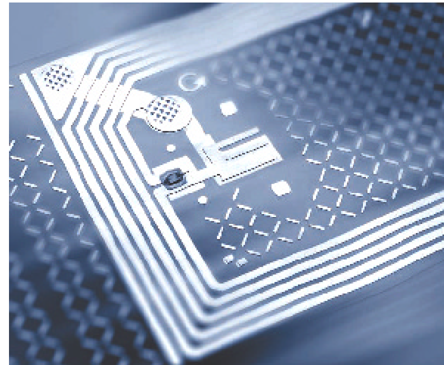
- easy field installation
- battery-free
- service-free

Self-powered Intelligent Sensor Systems
Smart Labels (Transponder)

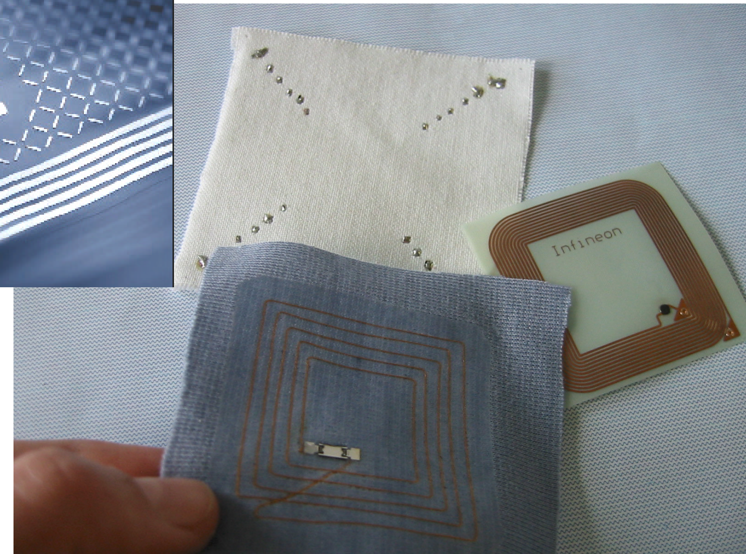
RF-ID tags for logistics in production, retailing and leasing



Magnetic Coupling



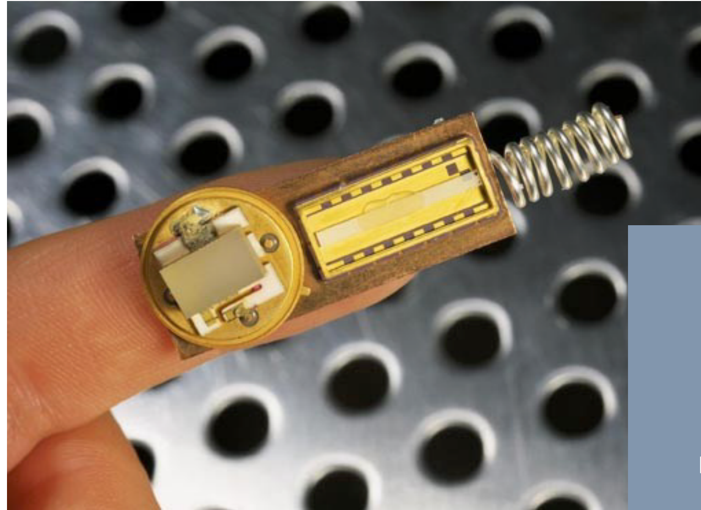
Infineon

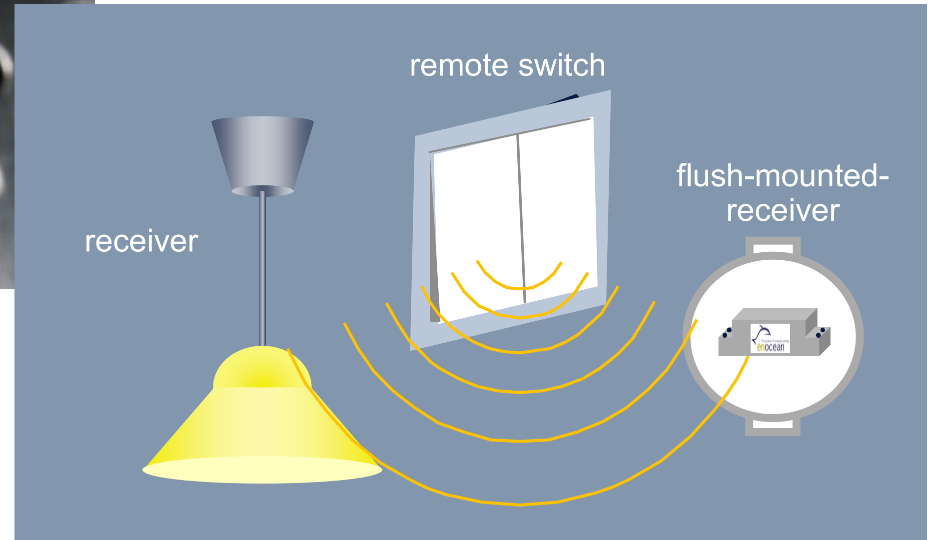


- low-cost
- passive
- data read- and writeable
- operation range 5 cm to 1 m

Self-powered Intelligent Sensor Systems
Piezoelectric Converter

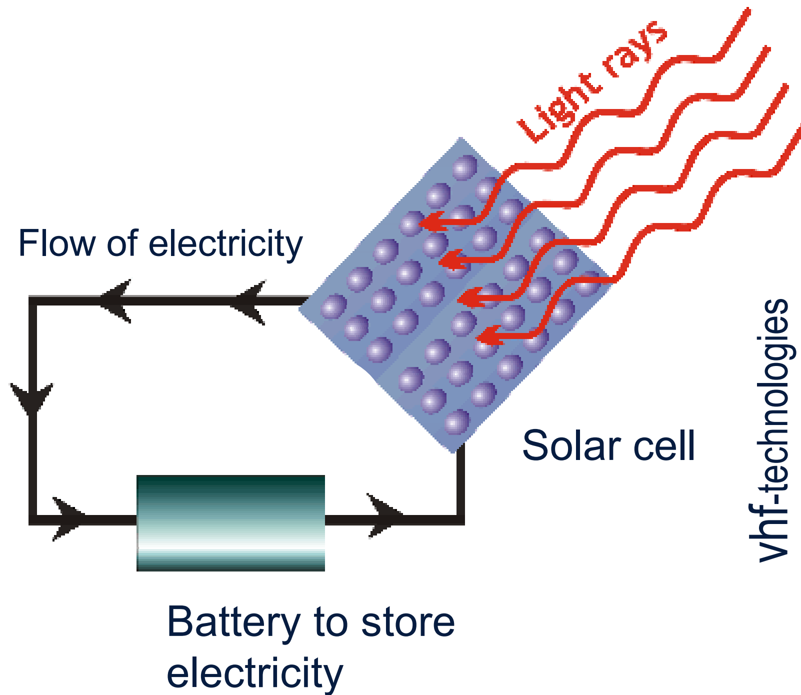
EnOcean

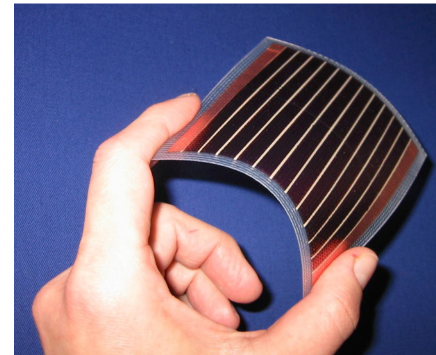




- Energy from sensed process sufficient for transmitting signals
- Ultra-low power processor and transmitter
- Radio link: 30 m operation range in buildings, 300 m in the open air

Ambient Energy Conversion
Energy from Light: Flexible Solar Cells





„flexcell"
thickness ≈0.6 mm
washable

Performance: power efficiency: 3%

@direct sun: ≈3 mW/cm²

@room light: ≈0.1 mW/cm²

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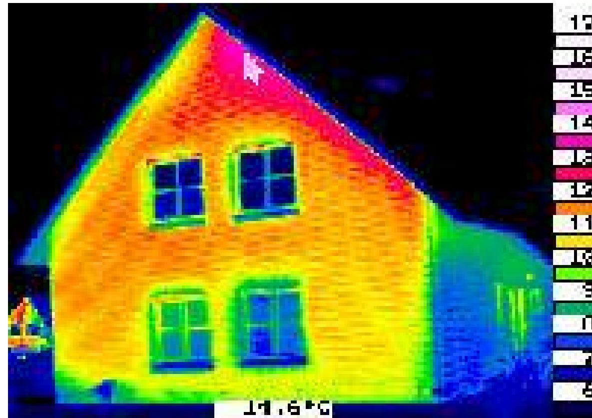
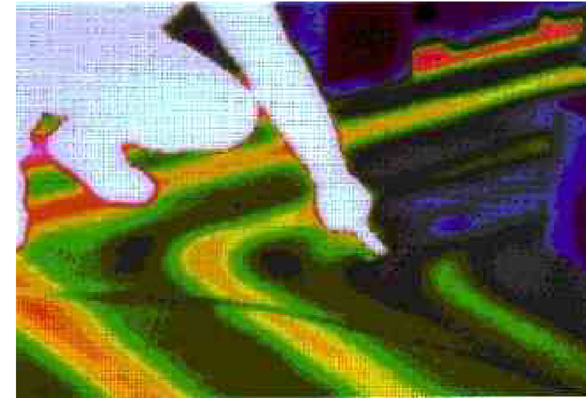
Ambient Energy Conversion
Temperature Differences in Our Environment



Building

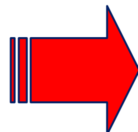


Thermografie-Büro
Heiling / Norden

Floor heating

Radiator

Car



Miniaturised thermogenerators convert a heat flux into electrical energy

Sönke Mehrgardt
Oldenburg

Ambient Energy Conversion
Thermoelectric Generator in CMOS

polysilicon
oxide
cavity
silicon substrate

CMOS chip integration

heat ejected
insulating plate
contact
n-type
p-type
P_{out}
heat input
electrical power output

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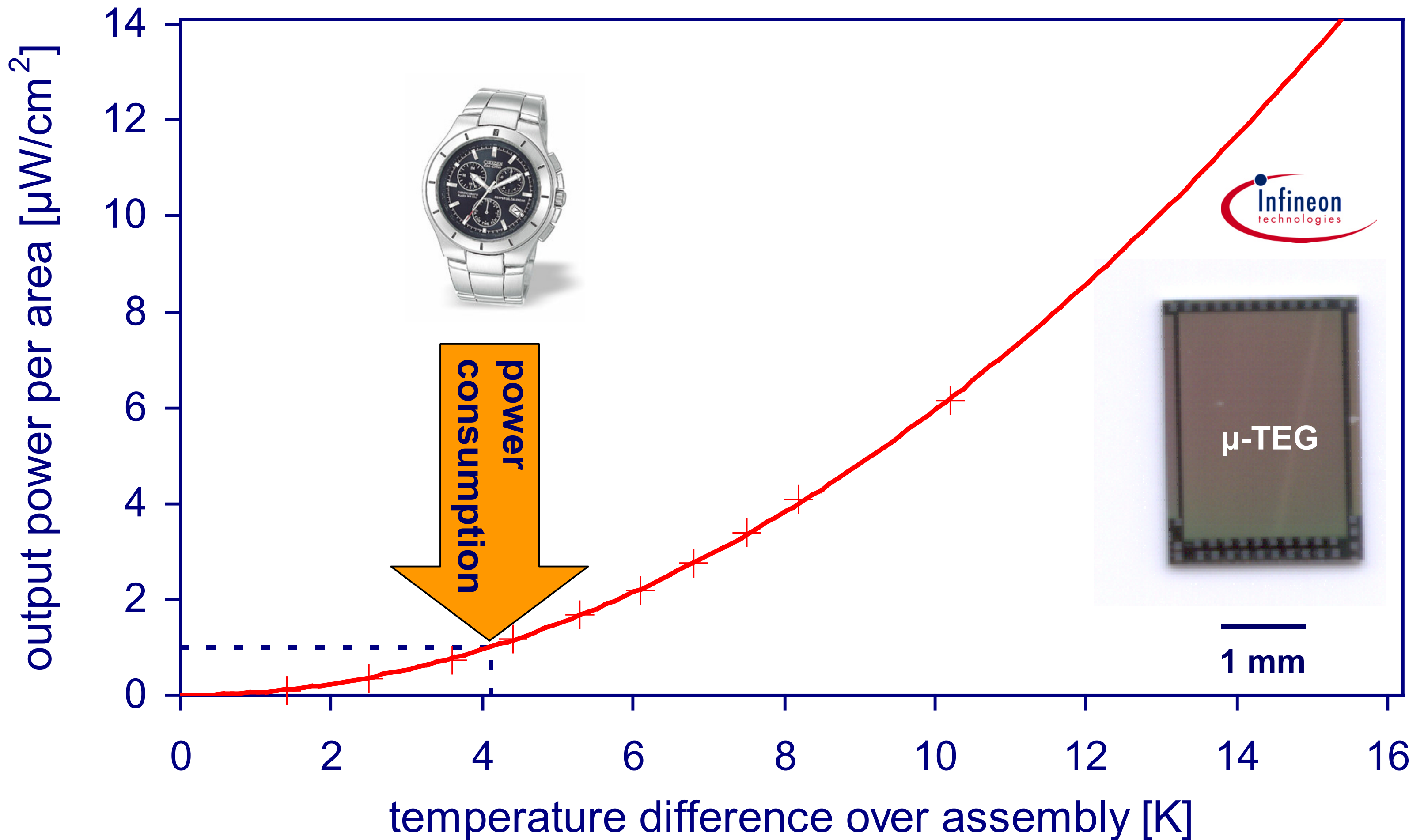
Ambient Energy Conversion
Thermogenerator in CMOS: Measured Output Power



Infineon technologies

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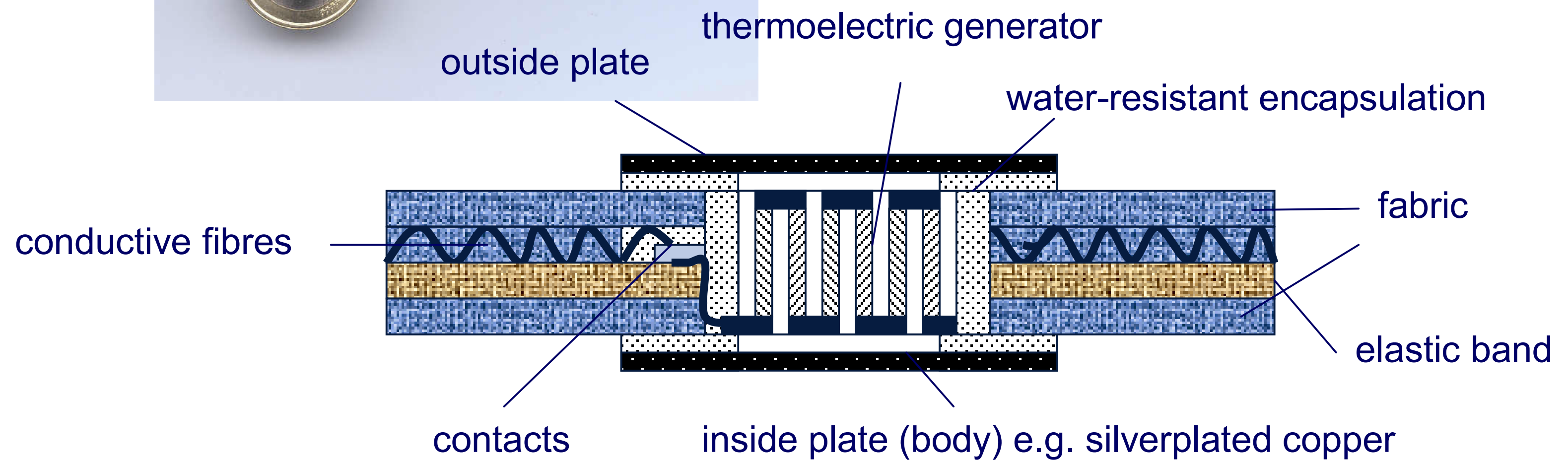
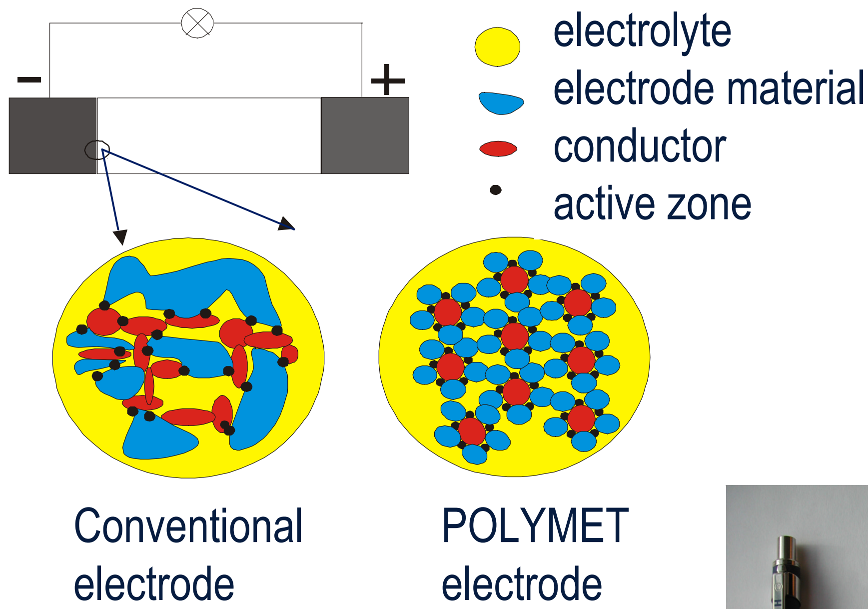
Ambient Energy Conversion
Textile Integration of Thermogenerators

thermogenerator integrated in textile fabric



Sönke Mehrgardt
Oldenburg
July 11th, 2003

Energy Storage: Textile Batteries



[POLY=]

polymere base

[=MET]

metal coated

→ very large electrode surface through textile structure

→ increased energy density (115Wh/kg)

→ battery thickness: ~0.3mm

"Never stop thinking"