High Level Tools for Low-Power ASIC design

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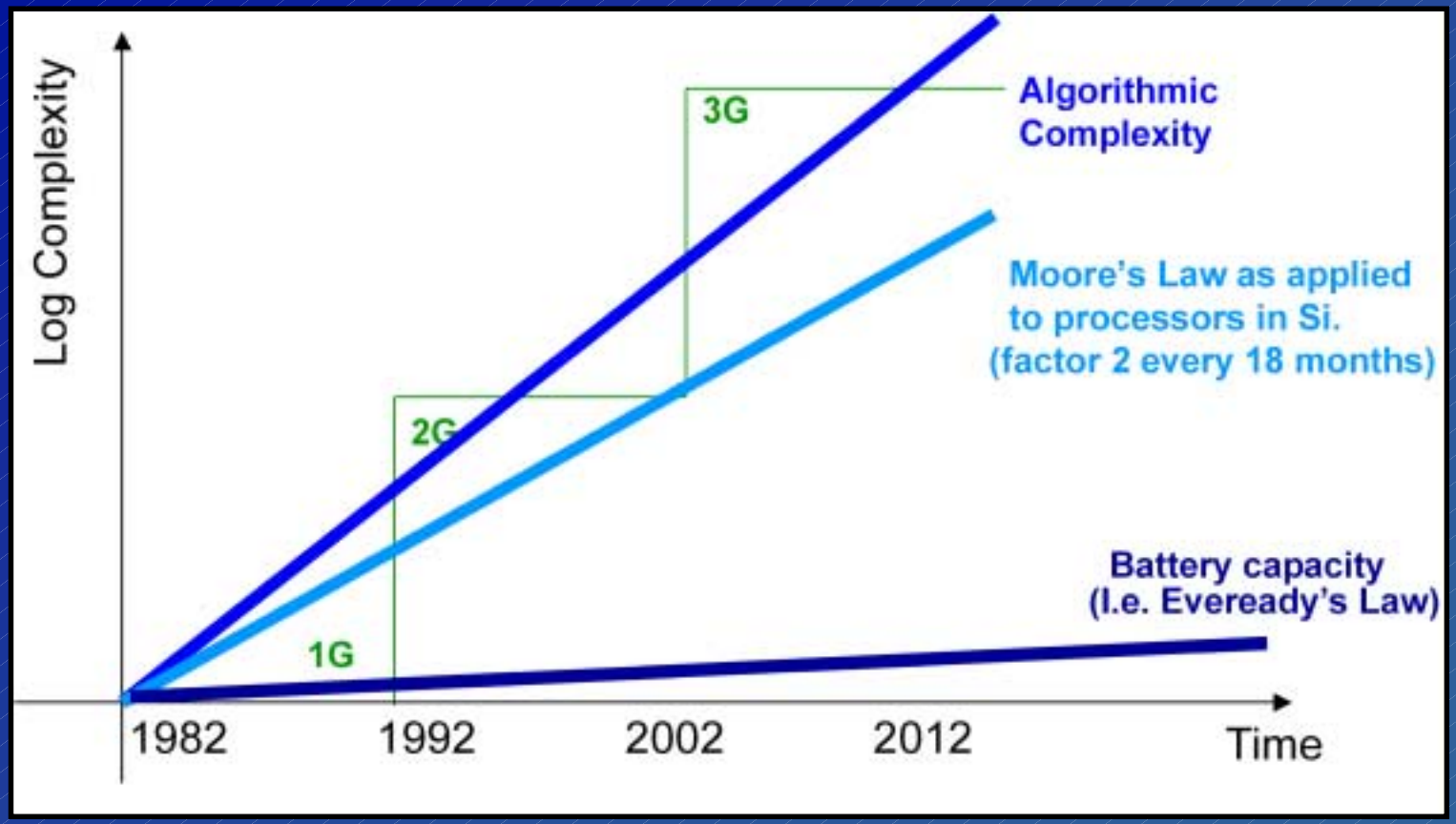
Overview

- introduction
- high level power estimation
  - µProcessors
  - ASICs
- tool overview
  - µProcessors
  - ASICs
- conclusion
- future work

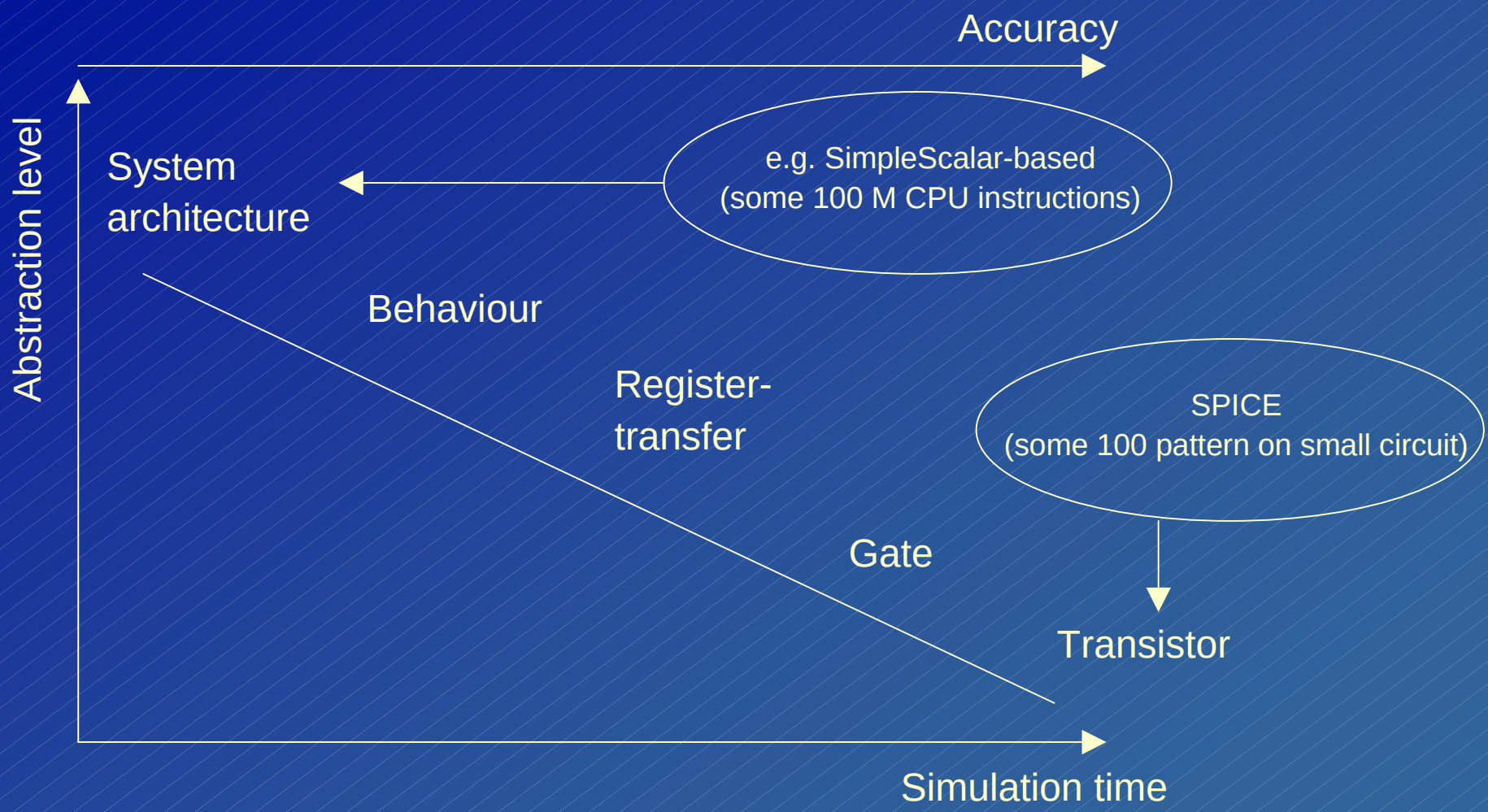
Moores Law



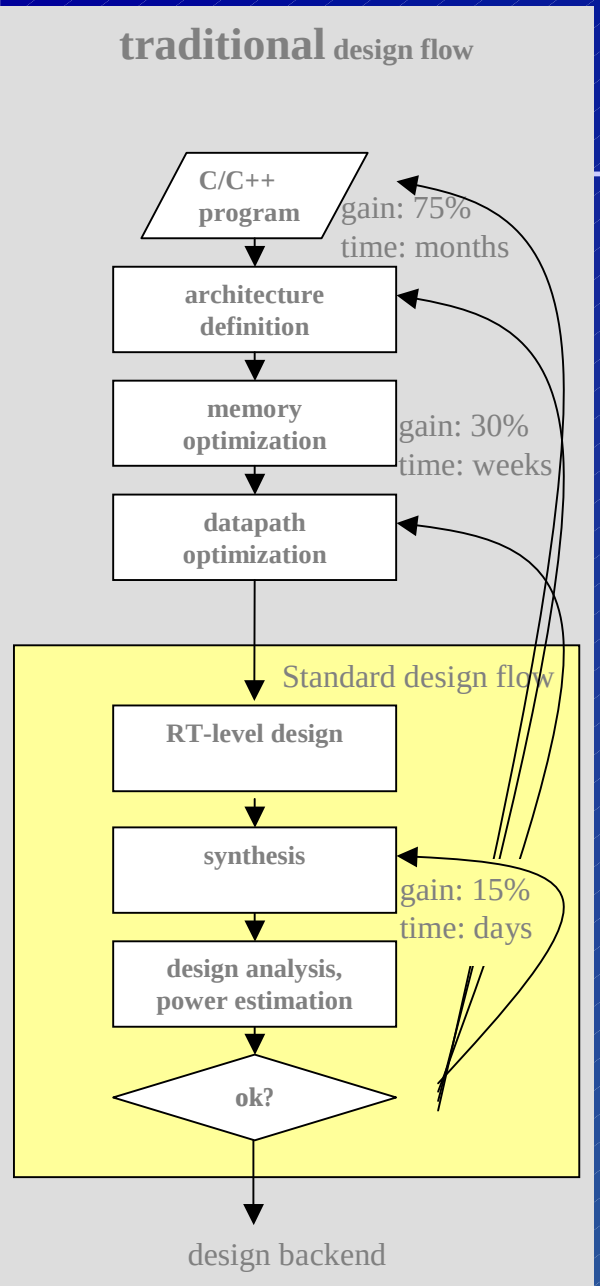
[Rab99]

- beating Moores Law

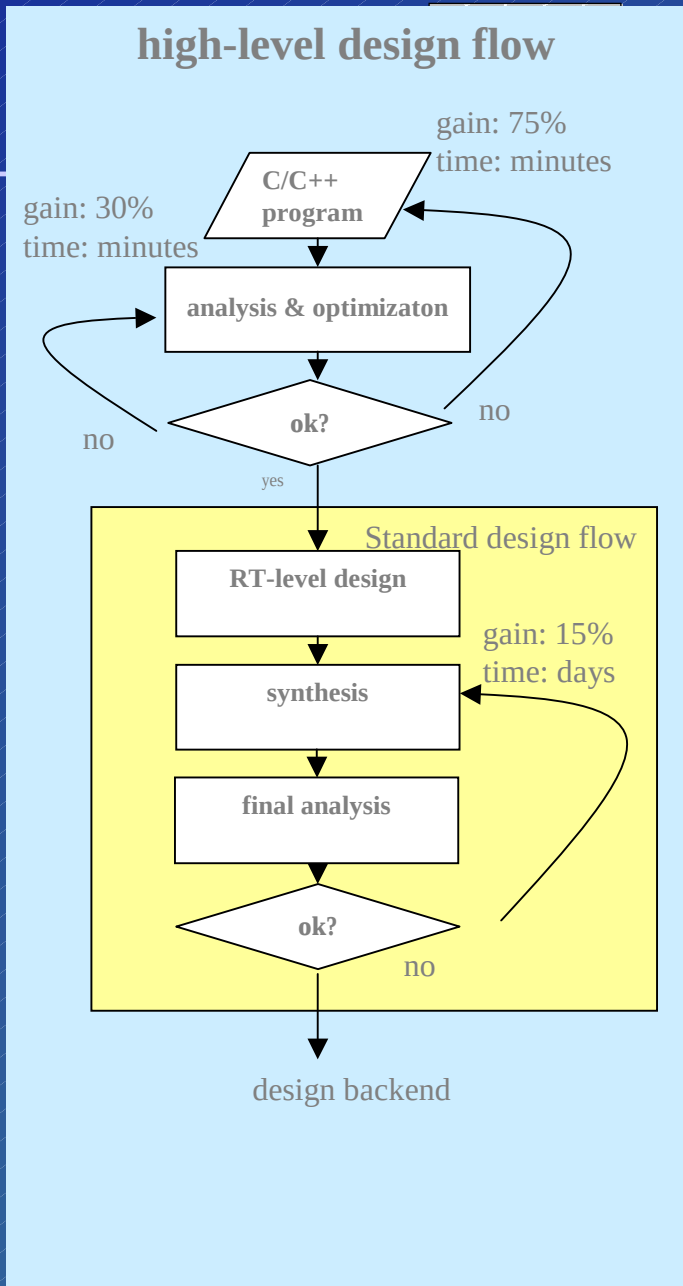
„Trade-off“


Accuracy
Abstraction level
System architecture
e.g. SimpleScalar-based
(some 100 M CPU instructions)
Behaviour
Register-transfer
SPICE
(some 100 pattern on small circuit)
Gate
Transistor
Simulation time

Why High-Level?



- specification level impact analysis.
- first time right architecture.
- up to 75% power reduction in minutes.
- avoids design iteration down to RT or gates.
- saves up to months of design time.



Embedded Approach

trend to software development:

- faster than hardware development
- cheaper than hardware development
- easier than hardware development
- updates/fixes are possible (e.g. firmware-updates)
- „off the shelf“ CPUs

➡ high-level power estimation for µ-Processors

➡ high-level power estimation for ASIC

Example SW Estimation Tool

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AccuPower overview:

- high level microprocessor power estimation tool
- contains
  - micro architectural simulators
  - library of VLSI layouts
  - power estimator
- based on SimpleScalar (MIPS-based ISA-simulator)
- vendor: academic

Algorithmic Level Estimation

two different approaches:

- quick synthesis to RTL net list
  - complex and slow
  - inaccurate if synthesis result does not get close to final architecture
    - internal information about applied synthesis tool necessary
- complexity analysis of control data flow graph (CDFG) representation
  - only transformation of algorithm into CDFG needed (compilation)
  - fast but less accurate
  - example: register power is computed by counting number of CDFG edges between operations

Example: Quick Synthesis Approach

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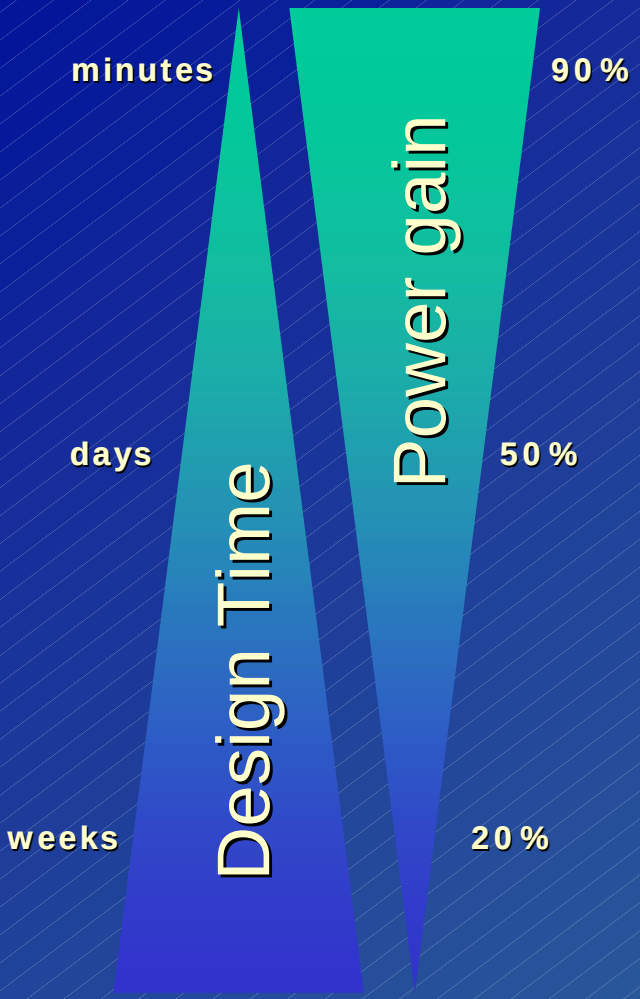
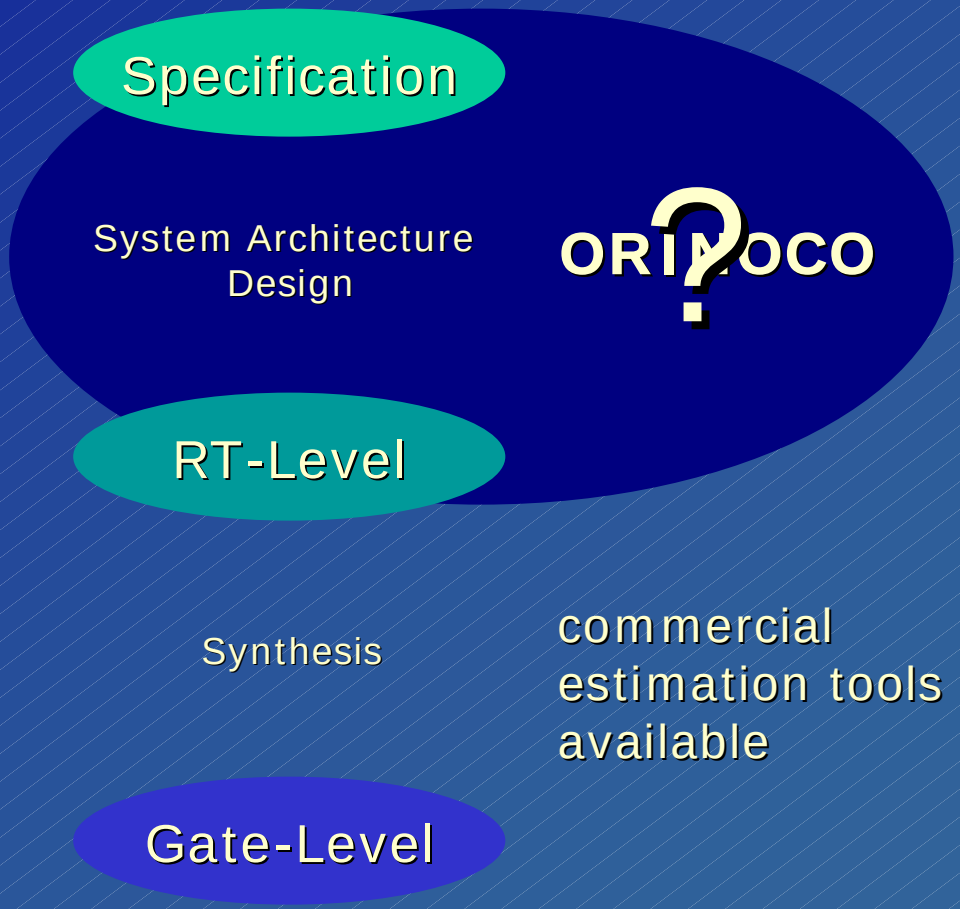
HyPE: Overview

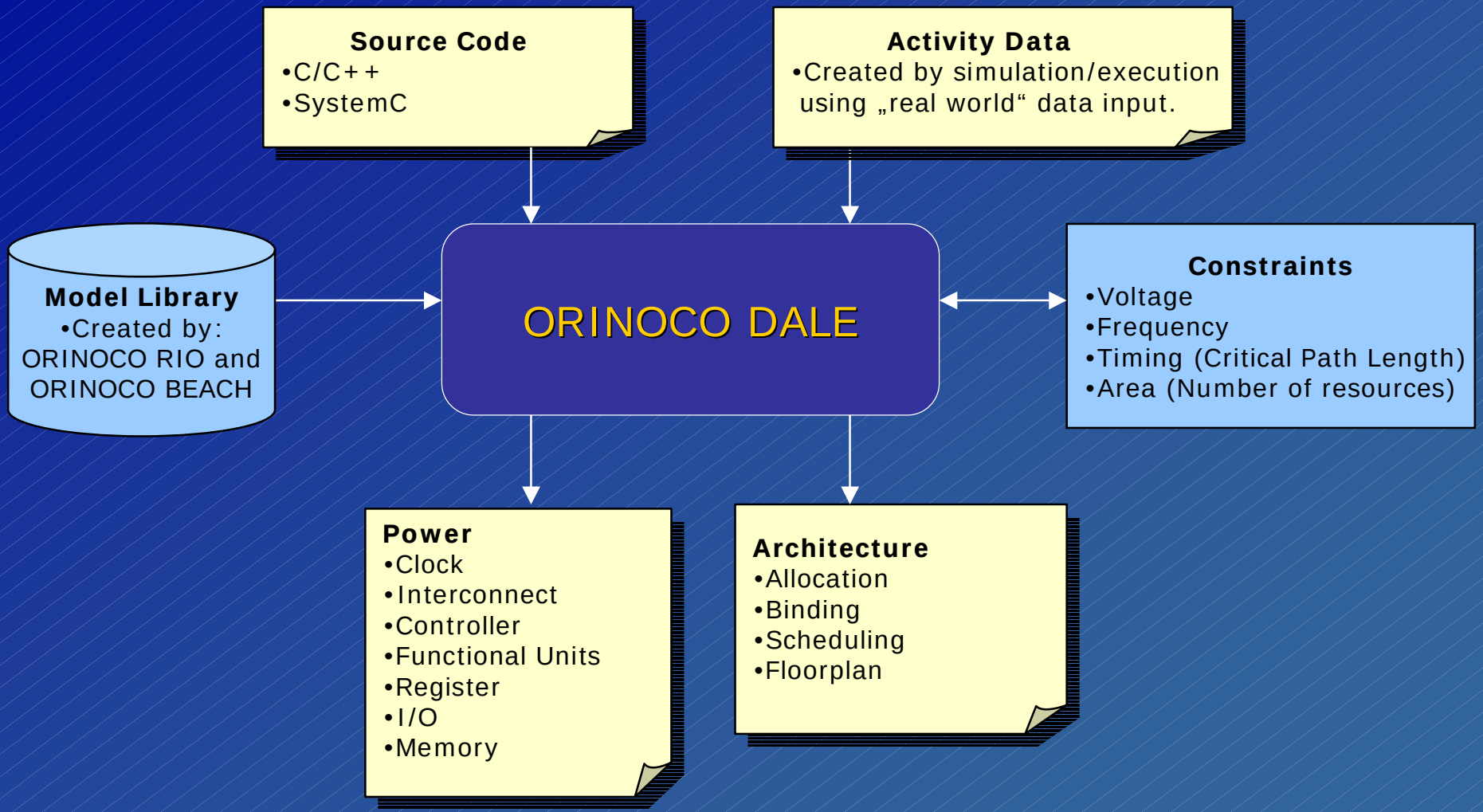
- Hybrid Power Estimation
- uses behavioural simulation and macro models for data path components
- three phases of estimation:
  - high level simulation
  - calculation of data path modes
  - statistical power estimation
- very high performance
- vendor: academic

Less Time to Low Power

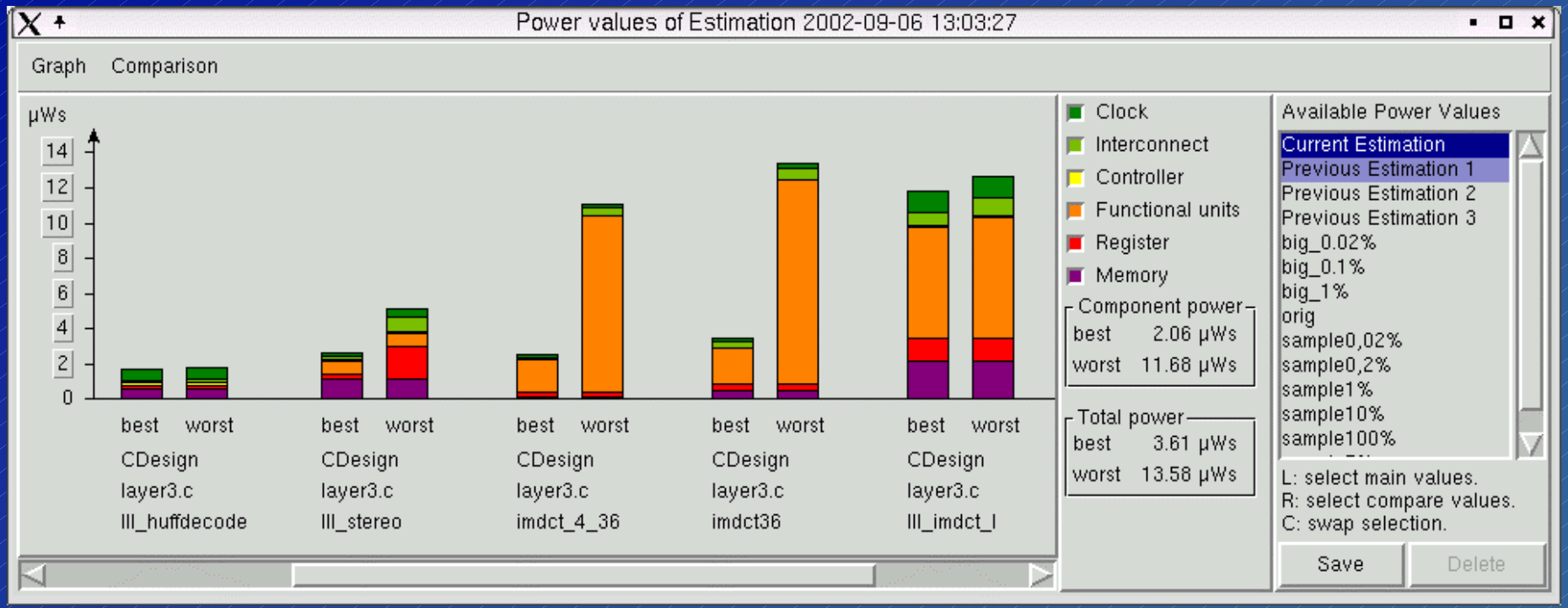




ORINOCO Principle



Example Estimation Result



Conclusion

- high-level power estimation: biggest gain is possible
- academic approaches for high-level power optimisation – leading edge of current research
- embedded software power estimation still research topic
- ASIC power estimation on lower levels: commercial tools available (eg. Synopsys, Sequence, Cadence)
- for higher levels first available tool: ORINOCO from ChipVision

Future Work

- research at OFFIS (SAO-group)
  - new metrics (interconnect, area, timing)
  - improved models (IP, leakage)
  - software power estimation (µ-Processors, partitioning)

- commercial exploitation at ChipVision Design Systems